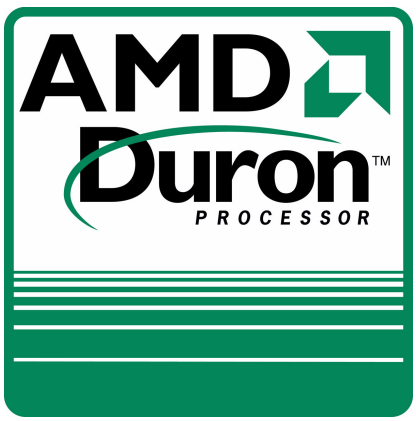
Preliminary Release

Mobile AMD Duron™ Processor

Model 7 Data Sheet



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Revision History

Date	Rev	Description
December 2001	F	Updated data sheet for the 1.0 GHz AMD Duron Processor Model 7 release. Revised the following sections: ■ Table 3, "Thermal Design Power," on page 31 ■ Table 8, "Valid Voltage and Frequency Combinations," on page 36 ■ Table 11, "VCC_CORE Voltage and Current," on page 40 ■ "Ordering Information" on page 85
November 2001	E	Revised "Thermal Protection Characterization" on page 49.
November 2001	D	Updated data sheet for the 950 MHz AMD Duron Processor Model 7 release. Revised the following sections: ■ "Processor Performance States and the FID_Change Protocol" on page 12 ■ "SYSCLK Multipliers" on page 24 ■ "Thermal Diode Characteristics" on page 48 ■ Figure 13, "Signal Relationship Requirements During Power-Up Sequence" on page 53 ■ "Power-Up Timing Requirements" on page 54 ■ "Clock Multiplier Selection (FID[3:0])" on page 56 Added the following sections and figures: ■ "Open Drain Test Circuit" and Figure 12, "General ATE Open Drain Test Circuit" on page 47. ■ "Thermal Protection Characterization" on page 49 and Table 18, "Guidelines for Platform Thermal Protection of the Processor," on page 51
September 2001	C	Updated Figure 9 on page 38.
August 2001	B	Initial public release.

1 Overview

The Mobile AMD Duron™ Processor Model 7 enables an optimized PC solution for value-conscious business and home users by providing the capability and flexibility to meet their computing needs for both today and tomorrow.

The mobile AMD Duron™ processor model 7 is the latest offering from AMD designed for the value segment of the notebook PC market. The innovative design was developed to accommodate new and more advanced applications, meeting the requirements of today's most demanding value-conscious buyers without compromising their budget. Model 7 is the CPU model number returned by the CPUID instruction for this processor. See Chapter 5, “CPUID Support” on page 29 for more information.

Delivered in a CPGA package, the mobile AMD Duron processor model 7 is the new AMD workhorse processor for value notebook systems, delivering high performance integer, floating-point and 3D multimedia capabilities for applications running on notebook PC platforms. The mobile AMD Duron processor model 7 provides value-conscious customers with access to advanced technology that allows their system investment to last for years to come.

Whether at work or at play, the mobile AMD Duron processor model 7 provides an optimum balance of performance and value for today’s advanced operating system software, business productivity applications, Internet computing and digital entertainment.

The mobile AMD Duron processor model 7 features a seventh-generation microarchitecture with a full-speed integrated L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core of the processor includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, a 64-Kbyte on-chip L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering 4.0 gigaflops (Gflops) of single-precision and more than 2.0 Gflops of double-precision floating-point results at

1.0 GHz, for superior performance on numerically complex applications.

This processor incorporates AMD PowerNow!™ technology, enabling performance and power saving modes specifically for notebook designs and is available in a low-profile, lidless CPGA package.

The mobile AMD Duron processor model 7 microarchitecture incorporates AMD's 3DNow!™ Professional technology, a high-performance cache architecture, and the 200-MHz 1.6-Gigabyte per second AMD Duron system bus. The AMD Duron system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide a powerful, scalable bus architecture.

The mobile AMD Duron processor model 7 is binary-compatible with existing x86 software and substantially compatible with applications optimized for 3DNow! Professional, MMX™, and SSE instructions. AMD's 3DNow! Professional technology implemented in the mobile AMD Duron processor model 7 includes new integer multimedia instructions and software-directed data movement instructions to deliver exceptional performance in multimedia applications.

1.1 Mobile AMD Duron™ Processor Model 7 Upgrades Versus the Mobile AMD Duron™ Processor Model 3

The following features summarize the mobile AMD Duron processor model 7 feature upgrades and differences from the mobile AMD Duron processor model 3:

- AMD PowerNow! technology for improved battery life
  - Model Specific Registers (MSRs) and SOFTVID and FID control pins which are compatible with the mobile AMD Athlon™ processor model 6
  - Automatic load sense
- Redesigned core, optimized for lower power and improved frequency scalability
- On-die temperature sensing diode

1.2 Mobile AMD Duron™ Processor Model 7 Microarchitecture Summary

The following features summarize the mobile AMD Duron processor model 7 microarchitecture:

- Performance on demand and extended battery life specifically for notebook designs with AMD PowerNow! technology
- The industry's first nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), SSE, MMX, and 3DNow! Professional instructions
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- 3DNow! Professional technology with added instructions to enable improved integer math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications
- 200-MHz AMD Duron system bus for high-performance main memory access, multimedia, graphics, and I/O
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, on-chip 64-Kbyte L2 cache

The mobile AMD Duron processor model 7 delivers superior notebook PC system performance in a cost-effective, industry-standard Socket A compatible 462-pin CPGA package. Figure 1 shows a typical mobile AMD Duron processor model 7 system block diagram.

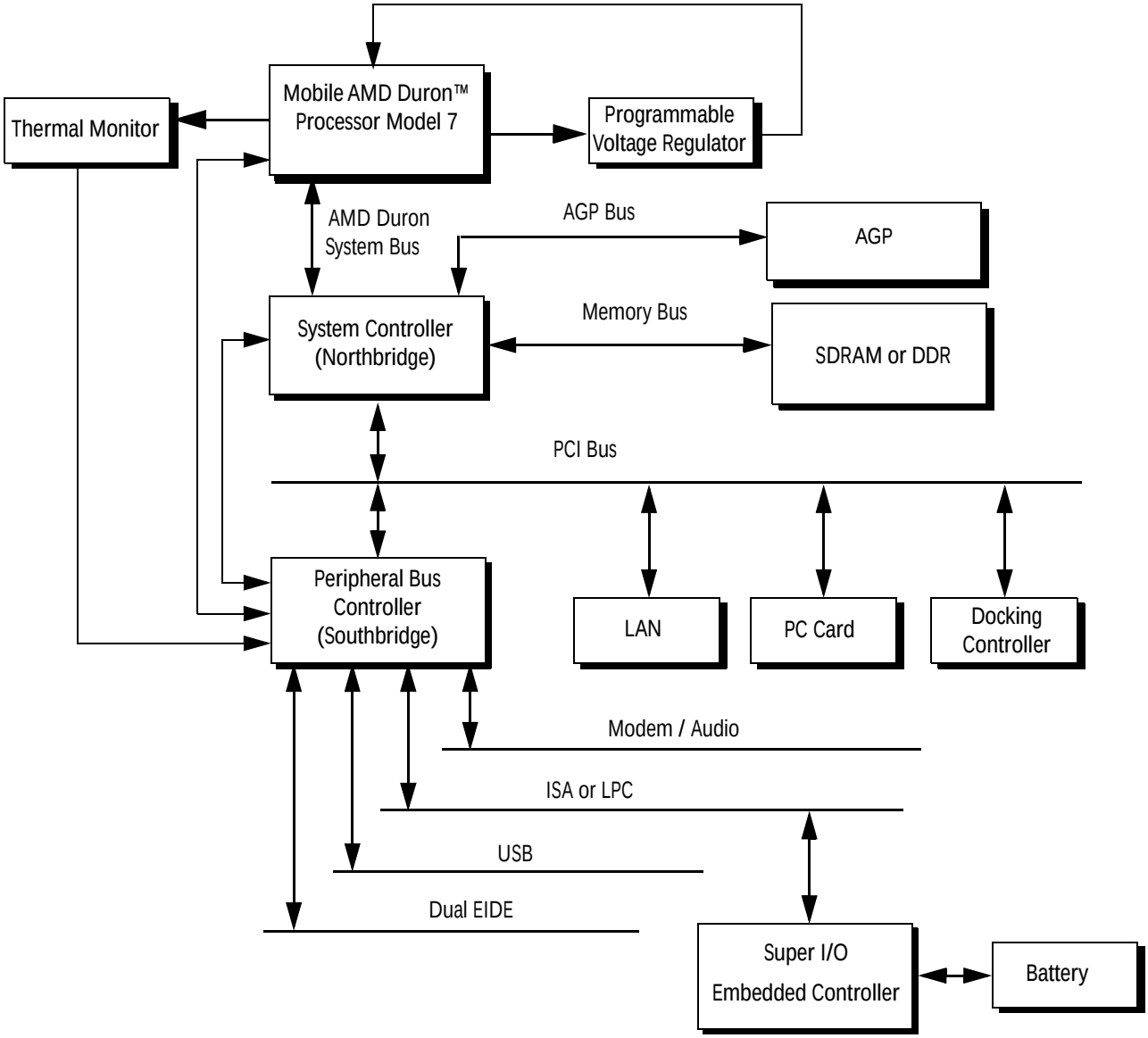


Figure 1. Typical Mobile AMD Duron™ Processor Model 7 System Block Diagram

2 Interface Signals

2.1 Overview

The AMD Duron™ system bus architecture is designed to deliver excellent data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull, low-voltage, swing-signaling technology contained within the Socket A socket.

For more information, see "AMD Duron™ System Bus Signals" on page 6, Chapter 10, "Pin Descriptions" on page 61, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD Duron system bus uses a low-voltage, swing-signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers that require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance-matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, "Pin Descriptions" on page 61.

2.3 Push-Pull (PP) Drivers

The mobile AMD Duron processor model 7 supports Push-Pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins.

See "ZN and ZP Pins" on page 83 for more information.

2.4 AMD Duron™ System Bus Signals

The AMD Duron system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, "Electrical Data" on page 33 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

Figure 2 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

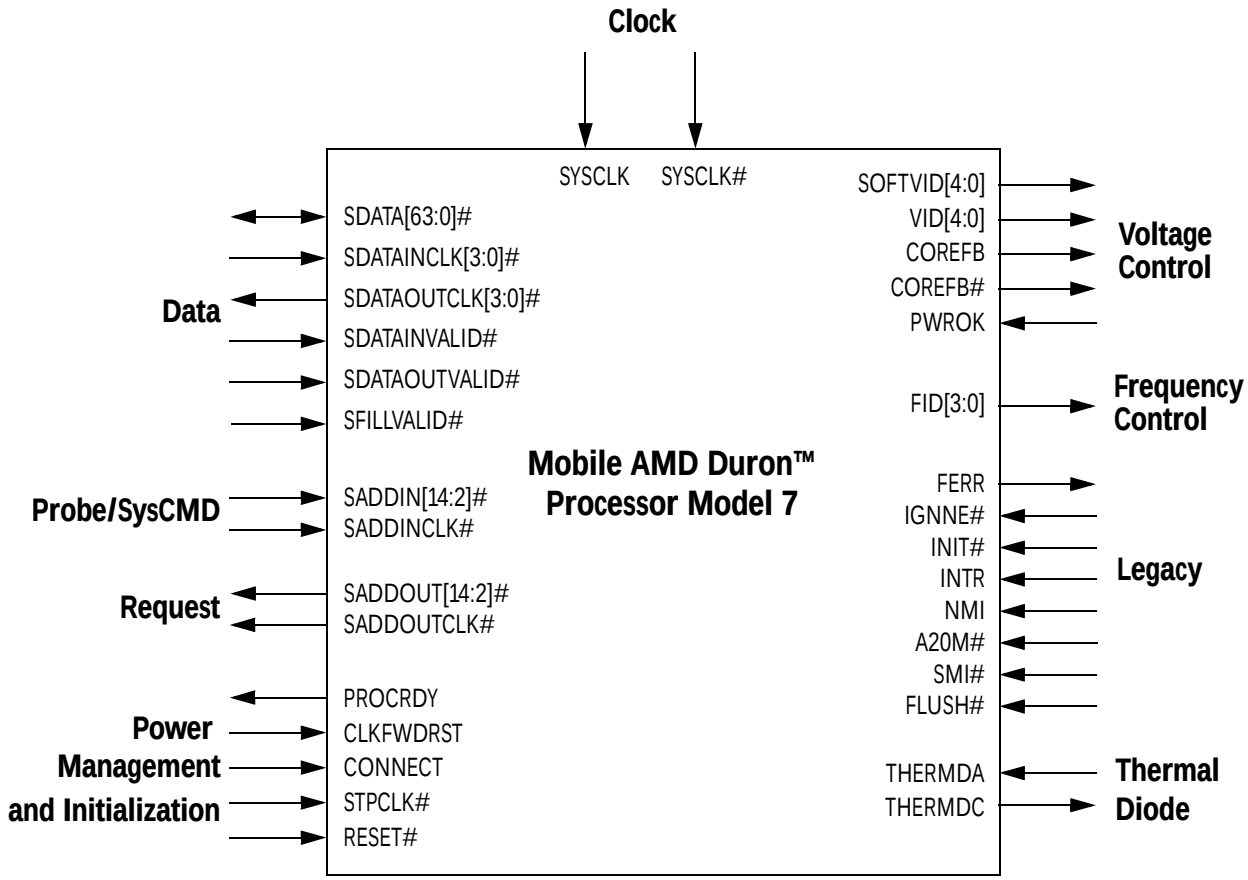


Figure 2. Logic Symbol Diagram

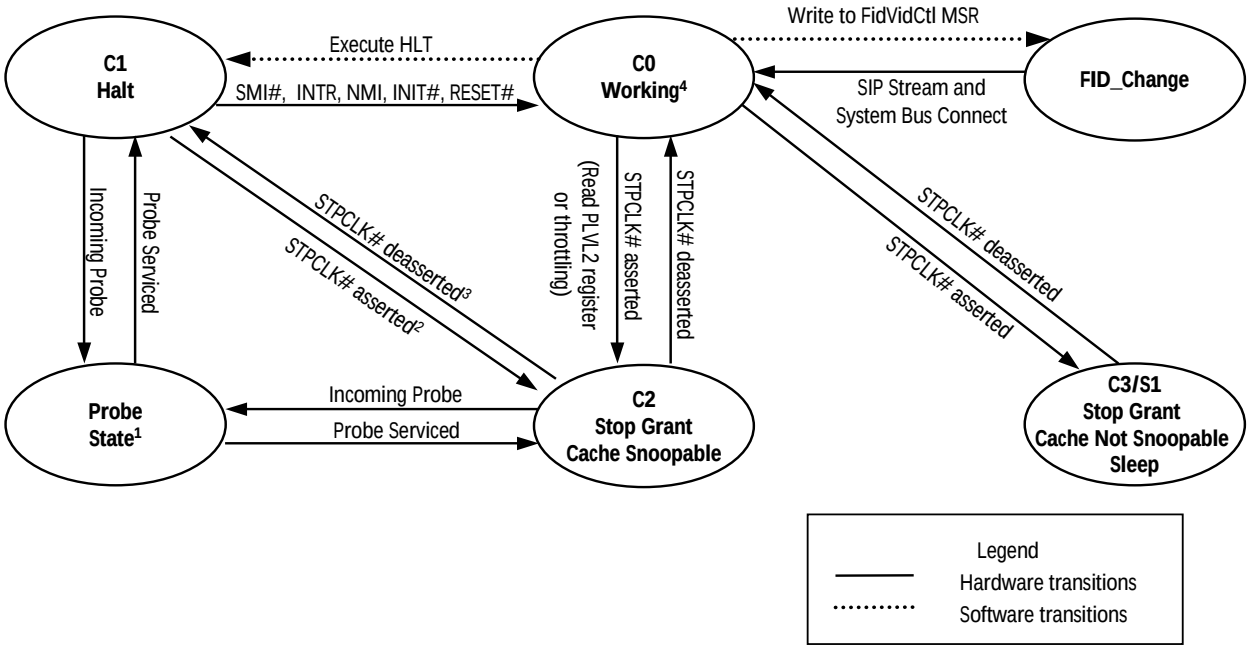
4 Power Management

This chapter describes the power management features of the mobile AMD Duron™ processor model 7. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications and support AMD PowerNow!™ technology.

4.1 Power Management States

The mobile AMD Duron™ processor model 7 has a variety of operating states that are designed to support different power management goals. In addition to the standard operating state, the processor supports low-power Halt and Stop Grant states and the FID_Change state. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems, for processor power management. AMD PowerNow! software is used to control processor performance states with operating systems that do not support ACPI 2.0-defined processor performance state control.

Figure 3 on page 10 shows the power management states of the processor. The figure includes the ACPI “Cx” naming convention for these states.



Note: The AMD Duron™ System Bus is connected during the following states:
1) The Probe state
2) During transitions between the Halt state and the C2 Stop Grant state
3) During transitions between the C2 Stop Grant state and the Halt state
4) C0 Working state

Figure 3. Mobile AMD Duron™ Processor Model 7 Power Management States

The following sections provide an overview of the power management states. For more details, refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

Note: *In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSCLK#) to the processor.*

Working State

The Working state is the state in which the processor is executing instructions.

Halt State

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Duron system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR if the system controller (Northbridge) disconnects the AMD Duron system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, INTR, NMI, RESET#, or SMI#. When the Halt state is exited the processor will initiate an AMD Duron system bus connect if it is disconnected.

Stop Grant States

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Duron system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR if the system controller (Northbridge) disconnects the AMD Duron system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, INTR, NMI, RESET#, or SMI#. When the Halt state is exited the processor will initiate an AMD Duron system bus connect if it is disconnected.

In C2, probes are allowed, as shown in Figure 3 on page 10.

The operating system places the processor into the C3 Stop Grant state by reading the P_LVL3 register in the Southbridge. In C3, the operating system and Northbridge hardware enforce a policy that prevents the processor from being probed. The Southbridge will deassert STPCLK# and bring the processor out of the C3 Stop Grant state if a bus master request, interrupt, or any other enabled resume event occurs.

The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP_TYP

and SLP_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 sleep state, system software ensures no bus master or probe activity occurs. The Southbridge deasserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

Probe State

The Probe state is entered when the Northbridge connects the AMD Duron system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD Duron system bus again.

FID_Change State

The FID_Change State is part of the AMD Duron system bus FID_Change Protocol. During the FID_Change state the Frequency Identification (FID[4:0]) code that determines the core frequency of the processor and Voltage Identification (VID[4:0]) driven on the SOFTVID[4:0] pins are transitioned to change the core frequency and core voltage of the processor.

Note: *The FID[3:0] pins of the processor do not transition as part of the FID_Change protocol.*

Processor Performance States and the FID_Change Protocol

The FID_Change protocol is used by AMD PowerNow! software to transition the processor from one performance state to another. The FID_Change protocol is also used for ACPI 2.0-compliant processor performance state control.

Processor performance states are combinations of processor core voltage and core frequency. Processor performance states are used in mobile systems to optimize the power consumption of the processor (and therefore battery powered run-time) based upon processor utilization.

See “Valid Voltage and Frequency Combinations” on page 36 for more information.

The core frequency is determined by a 5-bit Frequency ID (FID) code. The core voltage is determined by a 5-bit Voltage ID (VID) code.

- Before PWROK is asserted to the processor, the VID[4:0] outputs of the processor dictate the core voltage level of the processor.
- After PWROK is asserted, the core voltage of the processor is dictated by the SOFTVID[4:0] outputs. The SOFTVID[4:0] outputs of the processor are not driven to a deterministic value until after PWROK is asserted to the processor. The motherboard therefore must provide a 'VID Multiplexer' to drive the VID[4:0] outputs to the DC/DC converter for the core voltage of the processor before PWROK is asserted and drive the SOFTVID[4:0] outputs to the DC to DC converter after PWROK is asserted.
- The FID[3:0] signals are valid after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid.
- After RESET# is deasserted, the FID[3:0] outputs are not used to transmit FID information for subsequent software controlled changes in the operating frequency of the processor.
- Processor performance state transitions are required to occur as two separate transitions. The order of these transitions depends on whether the transition is to a higher or lower performance state. When transitioning from a lower performance state to a higher performance state the order of the transitions is:

  1. The FID_Change protocol is used to transition to the higher voltage, while keeping the frequency fixed at the current setting.
  2. The FID_Change protocol is then used to transition to the higher frequency, while keeping the voltage fixed at the higher setting.

  When transitioning from a high performance state to a lower performance state the order of the transitions is:

  1. The FID_Change protocol is used to transition to the lower frequency, while keeping the voltage fixed at its current setting.
  2. The FID_Change protocol is then used to transition to the lower voltage, while keeping the frequency fixed at the lower setting.
- The processor provides two MSRs to support the FID_Change protocol: the FidVidCtl MSR and the

FidVidStatus MSR. For a definition of these MSRs and their use, refer to the *Mobile AMD Athlon™ and Mobile AMD Duron™ Processors BIOS Developers Application Note*, order# 24141.

FID_Change Protocol Description By Example:

Note: *In any FID_Change transition only the core voltage or core frequency of the processor is transitioned. Two FID_Change transitions are required to transition the voltage and frequency to a valid performance state. When the voltage is being transitioned, the frequency is held constant by transitioning to the same FID[3:0] as the current FID reported in the FidVidStatus MSR.*

For detailed information on the optimized voltage and frequency combinations, see "Valid Voltage and Frequency Combinations" on page 36.

- System software determines that a change in processor performance state is required.
- System software executes a WRMSR instruction to write to the FidVidCtl MSR to dictate:
  - The new VID[4:0] code that will be driven to the DC/DC converter from the SOFTVID[4:0] outputs of the processor that selects the new core voltage level.
  - The new FID[4:0] code that will be used by the processor to dictate its new operating frequency.
  - A Stop Grant Timout Count (SGTC)[19:0] value that determines how many SYSCLK/SYSCLK# 100-MHz clock periods the processor will remain in the FID_Change state. This time accounts for the time that it takes for the PLL of the processor to lock to the new core frequency and the time that it takes for the core voltage of the processor to ramp to the new value.
  - The FIDCHGRATIO bit must be set to 1.
  - The VIDC bit must be set to a 1 if the voltage is going to be changed.
  - The FIDC bit must be set to a 1 if the frequency is going to be changed.

  Writing the SGTC field to a non-zero value initiates the FID_Change protocol.

- On the instruction boundary that the SGTC field of the FidVidCtl MSR is written to a non-zero value, the processor stops code execution and issues a FID_Change special cycle on the AMD Duron system bus.
- The FID_Change special cycle has a data encoding of 0007_0002h that is passed on SDATA[31:0].
- SDATA[36:32] contain the new FID[4:0] code during the FID_Change special cycle. The Northbridge is required to capture this FID[4:0] code when the FID_Change special cycle is run.
- In response to receiving the FID_Change special cycle, the Northbridge is required to disconnect. The Northbridge will complete any in-progress bus cycles and then disable its arbiter before disconnecting the AMD Duron system bus so that it will not initiate a AMD Duron system bus connect based on bus master or other activity. The Northbridge must disconnect the AMD Duron system bus or the system will hang because the processor is not executing any operating system or application code and is waiting for the AMD Duron system bus to disconnect so that it can continue with the FID_Change protocol. The Northbridge initiates an AMD Duron system bus disconnect in the usual manner: it deasserts CONNECT.
- The processor allows the disconnect to complete by deasserting PROCRDY. The Northbridge completes the disconnect by asserting CLKFWDRST.
- Once the AMD Duron system bus has been disconnected in response to a FID_Change special cycle, the Northbridge is not allowed to initiate a re-connect, the processor is responsible for the eventual re-connect.
- After the AMD Duron system bus is disconnected, the processor enters a low-power state where the clock grid is ramped down by a value specified in the CLK_Ctl MSR.
- After entering the low-power state, the processor will:
  - begin counting down the value that was programmed into the SGTC field
  - drive the new VID[4:0] value on SOFTVID[4:0], causing its core voltage to transition
  - drive the new FID[4:0] value to its PLL, causing the PLL to lock to the new core frequency.

- When the SGTC count reaches zero, the processor will ramp its entire clock grid to full frequency (the PLL is already locked to) and signal that it is ready for the Northbridge to transmit the new SIP (Serial Initialization Protocol) stream associated with the new processor core operating frequency. The processor signals this by pulsing PROCRDY high and then low.
- The Northbridge responds to this high pulse on PROCRDY by pulsing CLKFWDRST low and then transferring a SIP stream as it does after PROCRDY is deasserted after the deassertion of RESET#. The difference is that the SIP stream that the Northbridge transmits to the processor now corresponds to the FID[4:0] that was transmitted on SDATA[36:32] during the FID_Change special cycle.
- After the SIP stream is transmitted, the processor initiates the AMD Duron system bus connect sequence by asserting PROCRDY. The Northbridge responds by deasserting CLKFWDRST. The forward clocks are started and the processor issues a Connect special cycle.
- The AMD Duron system bus connection causes the processor to resume execution of operating system and application code at the instruction that follows the WRMSR to the FidVidCtl MSR that started the FID_Change protocol and processor performance state transition.

Figure 4 below illustrates the processor SOFTVID transition during the AMD Duron system bus disconnect in response to a FID_Change special cycle.

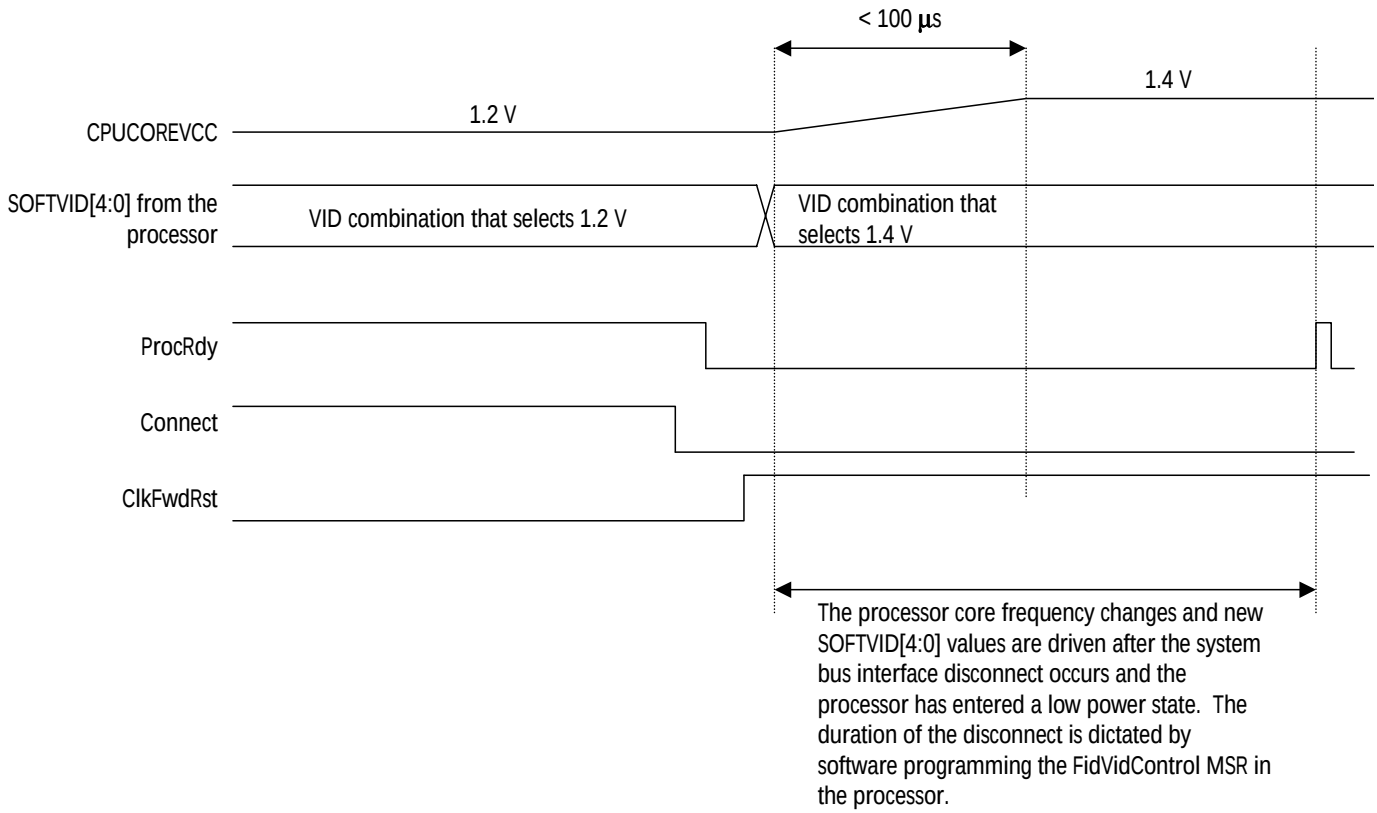


Figure 4. SOFTVID Transition During the AMD Duron™ System Bus Disconnect for FID_Change

4.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Duron system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a Connect special cycle.

AMD Duron system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt, Stop Grant, or FID_Change special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or completion of a FID_Change transition. Reconnect is initiated by the Northbridge to probe the processor. The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD Duron system bus before issuing the Stop Grant special cycle to the PCI bus or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted).

For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 5 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the AMD Duron system bus disconnected.

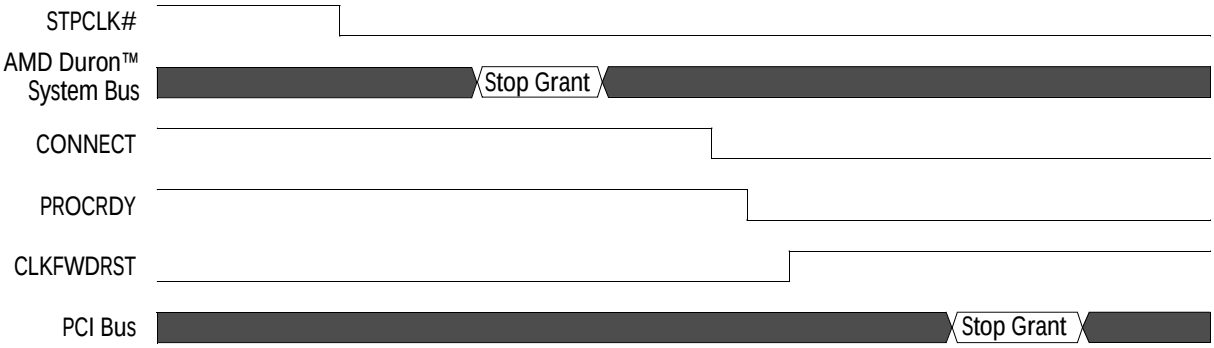


Figure 5. AMD Duron™ System Bus Disconnect Sequence in the Stop Grant State

An example of the AMD Duron system bus disconnect sequence is as follows:

1. The peripheral controller (Southbridge) asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, it enters the Stop Grant state and then issues a Stop Grant special cycle.
3. When the special cycle is received by the Northbridge, it deasserts CONNECT, assuming no probes are pending, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the processor enters a low-power state. The Northbridge passes the Stop Grant special cycle along to the Southbridge.

Figure 6 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD Duron system bus, and puts the processor into the Working state.

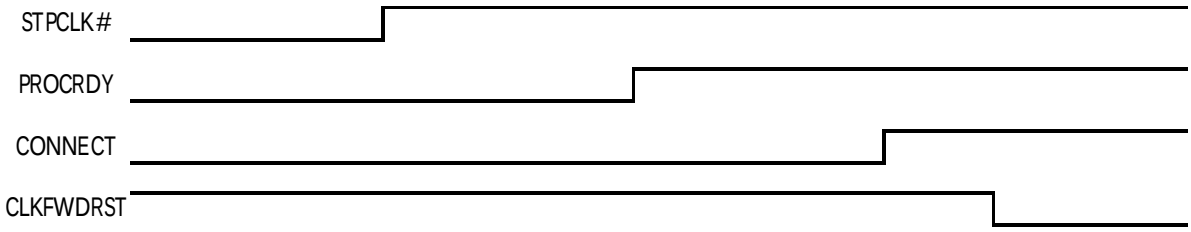


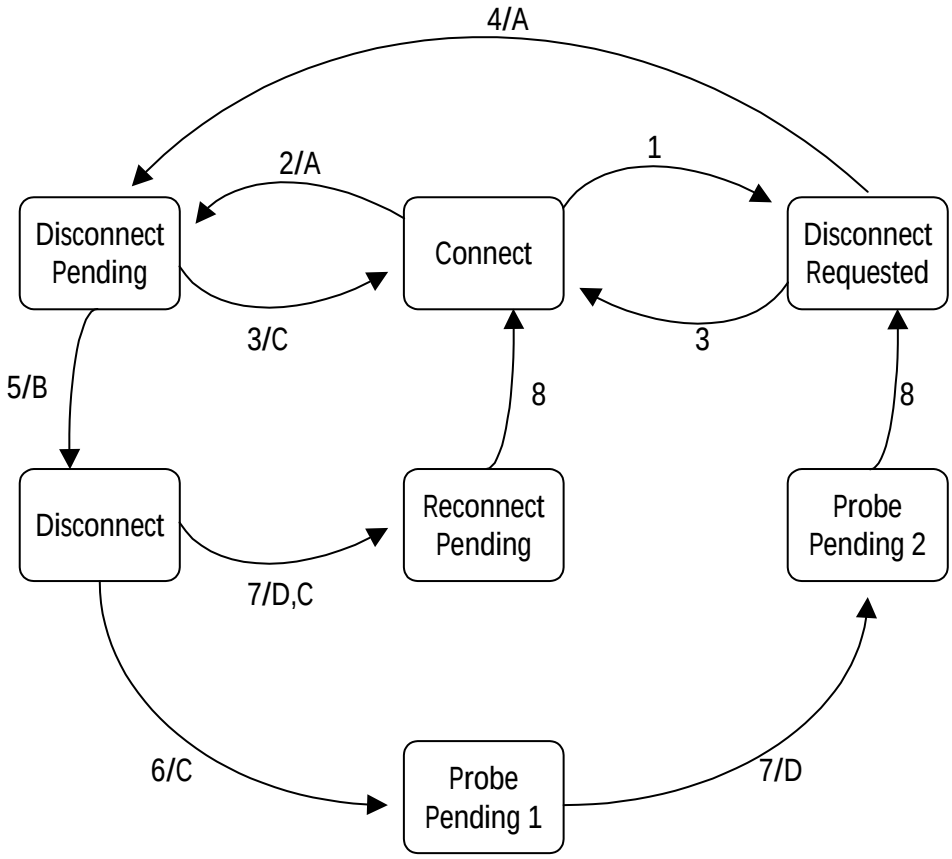
Figure 6. Exiting the Stop Grant State and Bus Connect Sequence

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1. The Southbridge deasserts STPCLK#, informing the processor of a wake event.
2. When the processor recognizes STPCLK# deassertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge deasserts CLKFWDRST, synchronizing the forwarded clocks between the processor and the Northbridge.
5. The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

Connect State Diagram

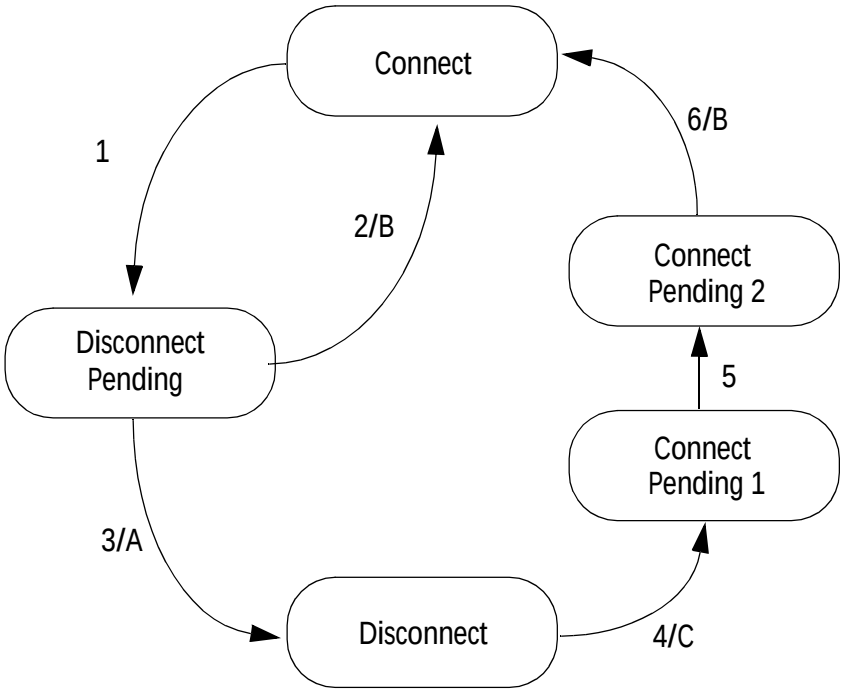
Figure 7 and Figure 8 on page 23 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is deasserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWDRST.
C	Assert CONNECT.
D	Deassert CLKFWDRST.

Figure 7. Northbridge Connect State Diagram



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is deasserted by the Northbridge.
6	Forward clocks start three SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a Connect special cycle.*
C	Return internal clocks to full speed and assert PROCRDY.

Note:

***** *The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Duron™ system bus is connected so the Northbridge can probe the processor, a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).*

Figure 8. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD Duron system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK_Ctl register.

4.4 SYSCLK Multipliers

The processor provides two mechanisms for communicating processor core operating frequency information to the Northbridge. These are the processor FID[3:0] outputs and the FID_Change special cycle. The FID[3:0] outputs specify the core frequency of the processor as a multiple of the 100-MHz input clock (SYSCLK/SYSCLK#) of the processor.

The FID[3:0] signals are valid after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid.The FID[3:0] outputs of the processor provide processor operating frequency information that the Northbridge uses when creating the SIP stream that the Northbridge sends to the processor after RESET# is deasserted. The FID[3:0] outputs always select a 5x SYSCLK multiplier:

```
FID[3:0] = 0 1 0 0
```

Software will use the FID_Change protocol to transition the processor to the desired performance state.

The FID[3:0] outputs are not used as part of the FID_Change protocol and do not change from their RESET# value during software-controlled processor core frequency transitions.

The FID_Change special cycle is used to communicate processor operating frequency information to the Northbridge during software-controlled processor core voltage and frequency (performance state) transitions. The FidVidCtl MSR allows software to specify a 5-bit FID value during software-controlled processor performance state transitions. The additional bit allows transitions to lower SYSCLK multipliers of 3x to 4x as well as all other SYSCLK multipliers supported by the processor.

For a description of the FID_Change protocol refer to the earlier section in this chapter.

Table 1 lists the FID[4:0] SYSCLK multiplier codes for the processor used by software to dictate the core frequency of the processor and the 5-bit value driven on SDATA[36:32]# by the processor during the FID_Change special bus cycle.

Note: *Only clock multipliers associated with operating frequencies specified in the* "Electrical Data" *chapter are valid for this processor.*

Note: *Software distinguishes the speed grade of the processor by reading the MFID field of the FidVidStatus MSR.*

Table 1. FID[4:0] SYSCLK Multiplier Combinations[1]

FID[4:0][2,3,5]	Clock Mode	SDATA[36:32]#[4]
00000	11x	11111
00001	11.5x	11110
00010	12x	11101
00011	12.5x	11100
00100	5x	11011
00101	5.5x	11010
00110	6x	11001
00111	6.5x	11000
01000	7x	10111
01001	7.5x	10110
01010	8x	10101
01011	8.5x	10100

Notes:

1. *On power up, the FID[3:0] balls are set to a clock multiplier value of 5x. After reset, software is responsible for transitioning the processor to the desired frequency.*
2. *Value programmed into the FidVidCtl MSR.*
3. *The maximum FID that may be selected by software is reported in the FidVidStatus MSR.*
4. *Value driven on SDATA[36:32]# balls during the FID_Change special bus cycle. The SDATA bus is active Low, so the SDATA[36:32]# values listed are what would be observed on the motherboard with a digital storage scope.*
5. *BIOS initializes the CLK_Ctl MSR to 6007_9263h during the POST routine. This CLK_Ctl setting is used with all FID combinations and selects a halt disconnect divisor of 128 and a Stop–Grant disconnect divisor of 512.*

Table 1. FID[4:0] SYSCLK Multiplier Combinations[1]

FID[4:0][2,3,5]	Clock Mode	SDATA[36:32]#[4]
01100	9x	10011
01101	9.5x	10010
01110	10x	10001
01111	10.5x	10000
10000	3x	01111
10001	Reserved	Reserved
10010	4x	01101
10011	Reserved	Reserved
10100	13x	11100
10101	13.5x	11100
10110	14x	11100
10111	Reserved	Reserved
11000	15x	11100
11001	Reserved	Reserved
11010	16x	11100
11011	16.5x	11100
11100	17x	11100
11101	18x	11100
11110	Reserved	Reserved
11111	Reserved	Reserved

Notes:

1. *On power up, the FID[3:0] balls are set to a clock multiplier value of 5x. After reset, software is responsible for transitioning the processor to the desired frequency.*
2. *Value programmed into the FidVidCtl MSR.*
3. *The maximum FID that may be selected by software is reported in the FidVidStatus MSR.*
4. *Value driven on SDATA[36:32]# balls during the FID_Change special bus cycle. The SDATA bus is active Low, so the SDATA[36:32]# values listed are what would be observed on the motherboard with a digital storage scope.*
5. *BIOS initializes the CLK_Ctl MSR to 6007_9263h during the POST routine. This CLK_Ctl setting is used with all FID combinations and selects a halt disconnect divisor of 128 and a Stop–Grant disconnect divisor of 512.*

4.5 Special Cycles

In addition to the special cycles documented in the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902, the processor supports the SMM Enter, SMM Exit, and FID_Change special cycles.

Table 2 defines the contents of SDATA[31:0] during the special cycles.

Table 2. Processor Special Cycle Definition

Special Cycle	Contents of SDATA[31:0]
SMM Enter	0005_0002h
SMM Exit	0006_0002h
FID_Change*	0007_0002h

Note:
* *The new FID[4:0] taken from the FID[4:0] field of the FidVidCtl MSR is driven on SDATA[36:32] during the FID_Change special cycle.*

5 CPUID Support

The mobile AMD Duron™ processor model 7 version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information about the CPUID features supported by the mobile AMD Duron processor model 7, refer to the following documents:

- *AMD Processor Recognition Application Note*, order# 20734

6 Thermal Design

The mobile AMD Duron™ processor model 7 provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor.

The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor.

Refer to "Thermal Diode Characteristics" on page 48 and "THERMDA and THERMDC Pins" on page 83 for more details.

For information about the usage of this diode and thermal design, including layout and airflow considerations, see the *Mobile System Thermal Design Guidelines,* order# 24383.

Table 3 shows the thermal design power.

Table 3. Thermal Design Power

Frequency (MHz)	Voltage	Thermal Design Power[1]
800	1.50 V	25 W
850	1.50 V	25 W
900	1.45 V	25 W
950	1.45 V	25 W
1000	1.40 V	25 W

Notes:

1. *Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal VCC_CORE. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature. Specified through characterization for a die temperature of 95°C.*

7 Electrical Data

7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group.

Table 4 defines each group and the signals contained in each group.

Table 4. Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], SOFTVID[4:0], VCCA, VCC_CORE, COREFB, COREFB#	See “” on page 38, “Soft Voltage Identification (SOFTVID[4:0])” on page 35, “VCCA AC and DC Characteristics” on page 35, “VCC_CORE AC and DC Characteristics” on page 37, “COREFB and COREFB# Pins” on page 78, “SOFTVID[4:0] and VID[4:0] Pins” on page 81, and “VCCA Pin” on page 83.
Frequency	FID[3:0]	See “Frequency Identification (FID[3:0])” on page 35 and “FID[3:0] Pins” on page 79.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK, PLLBYPASSCLK#,	See “SYSCLK and SYSCLK# AC and DC Characteristics” on page 41, “SYSCLK and SYSCLK#” on page 83, and “PLL Bypass and Test Pins” on page 80.

Table 4. Interface Signal Groupings (continued)

Signal Group	Signals	Notes
System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVALID#, SDATAINVALID#, SDATAOUTVALID#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD Duron™ System Bus AC and DC Characteristics" on page 43 and "CLKFWDRST Pin" on page 78.
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 45, "INTR Pin" on page 79, "NMI Pin" on page 80, "SMI# Pin" on page 81, "INIT# Pin" on page 79, "A20M# Pin" on page 78, "FERR Pin" on page 79, "IGNNE# Pin" on page 79, "STPCLK# Pin" on page 82, and "FLUSH# Pin" on page 79.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 45.
Test	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 45, "PLL Bypass and Test Pins" on page 80, "Scan Pins" on page 81, and "Analog Pin" on page 78,
Miscellaneous	DBREQ#, DBRDY, PWROK	See "General AC and DC Characteristics" on page 45, "DBRDY and DBREQ# Pins" on page 79, and "PWROK Pin" on page 80.
Reserved (RSVD)	Pins N1, N3, and N5	See "Reserved Pins DC Characteristics" on page 51, and "RSVD Pins" on page 80.
Thermal	THERMDA, THERMDC	See "Thermal Diode Characteristics" on page 48 and "THERMDA and THERMDC Pins" on page 83

7.3 Soft Voltage Identification (SOFTVID[4:0])

Table 5 shows the SOFTVID[4:0] DC Characteristics. For more information, see "SOFTVID[4:0] and VID[4:0] Pins" on page 81.

Table 5. SOFTVID[4:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
SOFTVID_V_{OH}	SOFTVID[4:0] Output High Voltage	–	2.625V *

Note:
* *The SOFTVID pins must not be pulled above this voltage by an external pullup resistor.*

7.4 Frequency Identification (FID[3:0])

Table 6 shows the FID[3:0] DC characteristics. For more information, see "FID[3:0] Pins" on page 79.

Table 6. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage	–	2.625 V *

Note:
* *The FID pins must not be pulled above this voltage by an external pullup resistor.*

7.5 VCCA AC and DC Characteristics

Table 7 shows the AC and DC characteristics for VCCA. For more information, see "VCCA Pin" on page 83.

Table 7. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{VCCA}	VCCA Pin Voltage (AC and DC)	2.25	2.5	2.75	V	1
I_{VCCA}	VCCA Pin Current	0		50	mA/GHz	2

Notes:
1. *Minimum and maximum voltages are absolute. No transients below minimum nor above maxiumum voltages are permitted.*
2. *Measured at 2.5 V.*

7.6 Decoupling

See the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the mobile AMD Duron™ processor model 7.

7.7 Valid Voltage and Frequency Combinations

Table 8 specifies the valid voltage and frequency combinations that this processor is characterized to operate. The Maximum Frequency column corresponds to the rated frequency of the processor. The Maximum FID (MFID) field in the FidVidStatus MSR is used by software to determine the maximum frequency of the processor. Each row in the table shows the maximum frequency allowable at the voltage specified in each column.

"Power Management" on page 9 describes how AMD PowerNow!™ software uses this information to implement processor performance states.

Table 8. Valid Voltage and Frequency Combinations

Maximum Frequency	VCC_CORE_NOM Voltage						
	1.50 V	1.45 V	1.40 V	1.35 V	1.30 V	1.25 V	1.20 V
800 MHz	800 MHz	700 MHz	650 MHz	600 MHz	550 MHz	500 MHz	≤ 500 MHz
850 MHz	850 MHz	750 MHz	700 MHz	650 MHz	600 MHz	550 MHz	≤ 500 MHz
900 MHz	N/A	900 MHz	800 MHz	750 MHz	700 MHz	650 MHz	≤ 550 MHz
950 MHz	N/A	950 MHz	850 MHz	800 MHz	750 MHz	700 MHz	≤ 600 MHz
1000 MHz	N/A	N/A	1000 MHz	900 MHz	850 MHz	800 MHz	≤ 700 MHz

Notes:

1. *All voltages listed are nominal.*
2. *The "≤" symbol indicates that any BIOS vendor can use any performance state equal to or less than the specified frquency at that given voltage. For example, "≤ 700 MHz" means that the BIOS may use 700 MHz, 600 MHz, 550 MHz, 500 MHz, 400 Mhz, or 300 Mhz provided that the chipset and system support the chosen processor operating frequencies.*
3. *The maximum processor die temperature is 95º C for all voltage and frequency combinations.*

7.8 VCC_CORE AC and DC Characteristics

Table 9 shows the AC and DC characteristics for VCC_CORE. For more information, see Table 24, "Cross-Reference by Pin Location," on page 70 and Figure 9 on page 38.

Table 9. VCC_CORE AC and DC Characteristics

Symbol	Parameter	Limit in Working State[2]	Units
$V_{CC\_CORE\_DC\_MAX}$	Maximum static voltage above $V_{CC\_CORE\_NOM}$[1]	100	mV
$V_{CC\_CORE\_DC\_MIN}$	Maximum static voltage below $V_{CC\_CORE\_NOM}$[1]	–50	mV
$V_{CC\_CORE\_AC\_MAX}$	Maximum excursion above $V_{CC\_CORE\_NOM}$[1]	150	mV
$V_{CC\_CORE\_AC\_MIN}$	Maximum excursion below $V_{CC\_CORE\_NOM}$ [1, 3]	–100	mV
t_{MAX_AC}	Positive excursion time for AC transients	10	µs
t_{MIN_AC}	Negative excursion time for AC transients	5	µs

Notes:

1. *VCC_CORE nominal values are shown in Table 8, "Valid Voltage and Frequency Combinations," on page 36.*
2. *All voltage measurements are taken differentially at the COREFB/COREFB# pins.*
3. *Absolute minimum allowable VCC_CORE voltage, including all transients, is 1.10 V.*

Figure 9 shows the processor core voltage (VCC_CORE) waveform response to perturbation. The t_{MIN_AC} (negative AC transient excursion time) and t_{MAX_AC} (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.

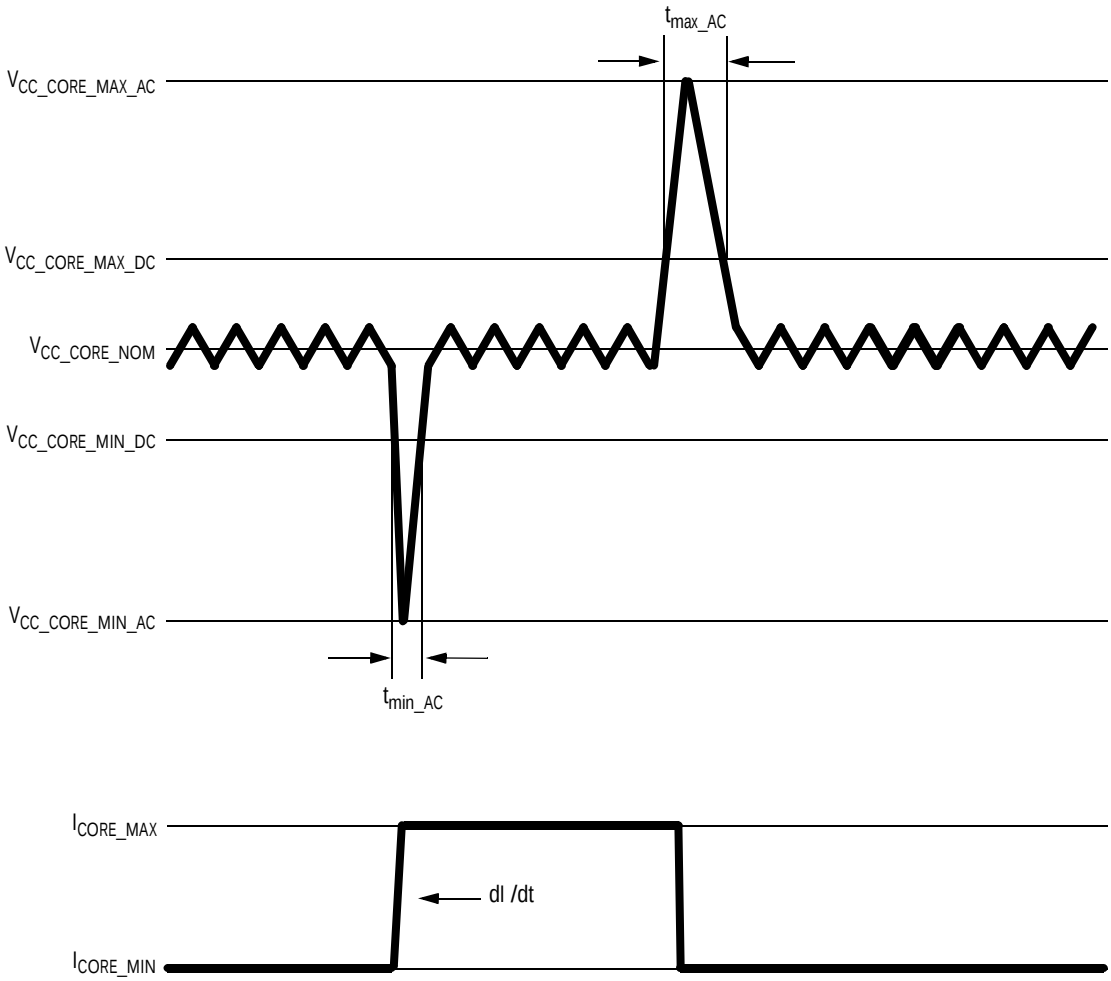


Figure 9. VCC_CORE Voltage Waveform

7.9 Absolute Ratings

Do not subject the processor to conditions that exceed the absolute ratings listed in Table 10, as such conditions may adversely affect long-term reliability or result in functional damage.

Table 10. Absolute Ratings

Parameter	Description	Min	Max
VCC_CORE	Mobile AMD Duron™ Processor Model 7 core supply	–0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Duron Processor Model 7 PLL supply	–0.5 V	VCCA Max + 0.5 V
V_{PIN}	Voltage on any signal pin	–0.5 V	VCC_CORE Max + 0.5 V
$T_{STORAGE}$	Storage temperature of processor	–40ºC	100ºC

7.10 VCC_CORE Voltage and Current

Table 11 shows the voltage and current of the processor during normal and reduced power states.

Table 11. VCC_CORE Voltage and Current

Frequency (MHz)	Nominal Voltage	Maximum I_{CC} (Power Supply Current)	Die Temperature	Notes
800	1.50 V	16.70 A	95°C	
850				
900	1.45 V	17.20 A		
950				
1000	1.40 V	17.90		
Halt/Stop Grant C2	1.20 V	2.00 A		1, 2, 3
Stop Grant C2		1.07 A	50°C	1, 2, 3, 4
Stop Grant C3/S1		0.80 A		1, 2, 3, 4

Notes:

1. *See also Figure 3, "Mobile AMD Duron™ Processor Model 7 Power Management States" on page 10.*
2. *The maximum Stop Grant currents are absolute worst case currents for parts that may yield from the worst case corner of the process, and are not representative of the typical Stop Grant current that is currently about one-third of the maximum specified current.*
3. *These currents occur when the AMD Duron system bus is disconnected and a low power ratio of 1/512 is applied to the core clock grid of the processor as dictated by a value of 6007_9263h programmed into the Clock Control (CLK_Ctl) MSR.*
4. *The Stop Grant current consumption is characterized and not tested.*

7.11 SYSCLK and SYSCLK# AC and DC Characteristics

Table 12 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together.

Table 12. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{Threshold-DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold-AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pullup to VCC_CORE	–250		µA
I_{LEAK_N}	Leakage current through N-channel pulldown to VSS (Ground)		250	µA
V_{CROSS}	Differential signal crossover		VCC_CORE/2 +/– 100	mV
C_{PIN}	Capacitance	4	12	pF

Figure 10 shows the DC characteristics of the SYSCLK and SYSCLK# signals.

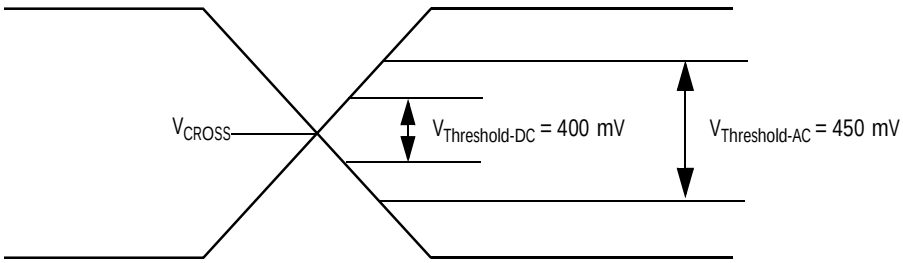


Figure 10. SYSCLK and SYSCLK# Differential Clock Signals

Table 13 shows the mobile AMD Duron processor model 7 SYSCLK/SYSCLK# differential clock AC characteristics.

Table 13. SYSCLK and SYSCLK# AC Characteristics

Symbol	Description	Min	Max	Units	Notes
	Clock Frequency	50	100	MHz	
	Duty Cycle	30%	70%	–	
t_1	Period	10		ns	1, 2
t_2	High Time	1.8		ns	
t_3	Low Time	1.8		ns	
t_4	Fall Time		2	ns	
t_5	Rise Time		2	ns	
	Period Stability		± 300	ps	

Notes:

1. *Circuitry driving the SYSCLK and SYSCLK# inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20 dB attenuation point, as measured into a 10-pF or 20-pF load must be less than 500 kHz.*
2. *Circuitry driving the SYSCLK and SYSCLK# inputs may purposely alter the SYSCLK and SYSCLK# period (spread spectrum clock generators). In no cases can the period violate the minimum specification above. SYSCLK and SYSCLK# inputs may vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.*

Figure 11 shows a sample waveform.

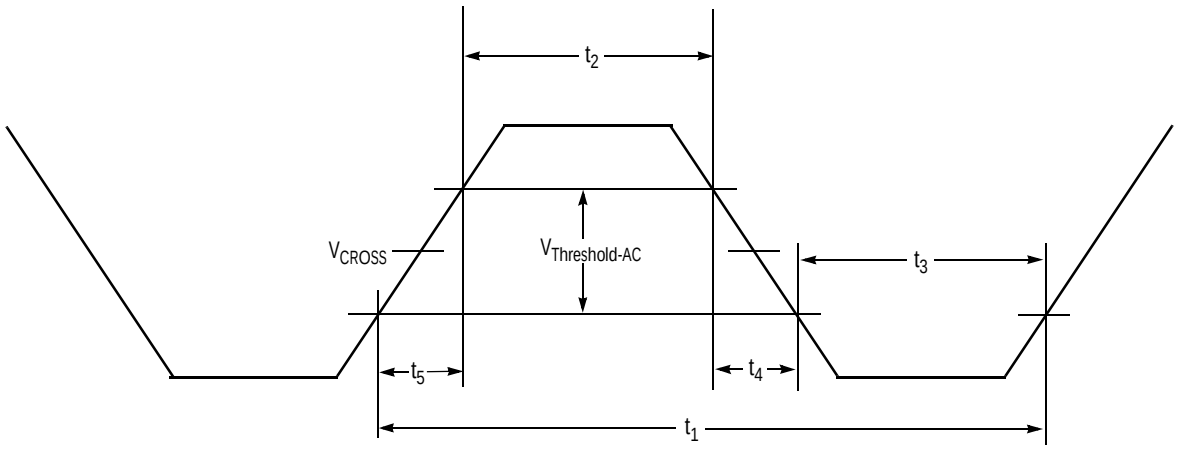


Figure 11. SYSCLK Waveform

7.12 AMD Duron™ System Bus AC and DC Characteristics

Table 14 shows the DC characteristics of the AMD Duron system bus.

Table 14. AMD Duron™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		(0.5 x VCC_CORE) –50	(0.5 x VCC_CORE) +50	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN}=V_{REFNominal}$	–100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN}=V_{REFNominal}$		+100	µA	
V_{IH}	Input High Voltage		V_{REF} + 200	VCC_CORE + 500	mV	
V_{IL}	Input Low Voltage		–500	V_{REF} – 200	mV	
V_{OH}	Output High Voltage	I_{OUT} = –200 µA	0.85*VCC_CORE	VCC_CORE+500	mV	2
V_{OL}	Output Low Voltage	I_{OUT} = 1 mA	–500	400	mV	2
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN}= VSS (Ground)	–250		µA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN}= VCC_CORE Nominal		+250	µA	
C_{IN}	Input Pin Capacitance		4	12	pF	

Notes:

1. *V_{REF}*
   – V_{REF} is nominally set by a (1%) resistor divider from VCC_CORE.
   – The suggested divider resistor values are 100 ohms over 100 ohms to produce a divisor of 0.50.
   – Example: VCC_CORE = 1.4 V, V_{REF} = 750 mV (1.4 x 0.50).
   – Peak-to-Peak AC noise on V_{REF} (AC) should not exceed 2% of V_{REF} (DC).
2. *Specified at T = 95°C and VCC_CORE.*

The AC characteristics of the AMD Duron system bus are shown in Table 15. The parameters are grouped based on the source or destination of the signals involved.

Table 15. AMD Duron™ System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	T_{SU}	Input Data Setup Time	300	–	ps	3
	T_{HD}	Input Data Hold Time	300	–	ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	4, 5
	T_{SU}	Setup to RSTCLK	500	–	ps	4, 6
	T_{HD}	Hold from RSTCLK	1000	–	ps	4, 6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, and CLKFWDRST.*
5. *T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25 pF.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

7.13 General AC and DC Characteristics

Table 16 shows the mobile AMD Duron processor model 7 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 16. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		(VCC_CORE/2) + 200mV	VCC_CORE Max	V	1, 2
V_{IL}	Input Low Voltage		–300	350	mV	1, 2
V_{OH}	Output High Voltage		VCC_CORE – 400	VCC_CORE + 300	mV	
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN}= VSS (Ground)	–250		µA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN}= VCC_CORE Nominal		250	µA	
I_{OH}	Output High Current			–16	mA	3
I_{OL}	Output Low Current		16		mA	3
T_{SU}	Sync Input Setup Time		2.0		ns	4, 5
T_{HD}	Sync Input Hold Time		0.0		ps	4, 5
T_{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T_{BIT}	Input Time to Acquire		20.0		ns	7, 8

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} maximum and V_{OH} minimum, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to enable capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*
14. *Time to valid is for any open drain pins. See requirements 7 and 8 in Chapter 8, "Power–Up Timing Requirements," for more information.*

Table 16. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T_{RPT}	Input Time to Reacquire		40.0		ns	9–13
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	6
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	6
C_{PIN}	Pin Capacitance		4	12	pF	
T_{VALID}	Time to data valid			100	ns	14

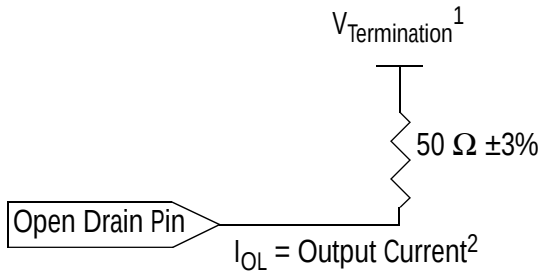
Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} maximum and V_{OH} minimum, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to enable capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*
14. *Time to valid is for any open drain pins. See requirements 7 and 8 in Chapter 8, "Power–Up Timing Requirements," for more information.*

7.14 Open Drain Test Circuit

Figure 12 is a test circuit that may be used on Automated Test Equipment (ATE) to test for validity on open drain pins.

Refer to Table 16, “General AC and DC Characteristics,” on page 45 for timing requirements.



Notes:

1. *$V_{Termination}$ = 1.2 V for VID and FID pins*
2. *I_{OL} = –16 mA for VID and FID pins*

Figure 12. General ATE Open Drain Test Circuit

7.15 Thermal Diode Characteristics

Thermal Diode Electrical Characteristics. Table 17 shows the mobile AMD Duron processor model 7 electrical characteristics of the on-die thermal diode.

Table 17. Thermal Diode Electrical Characteristics

Symbol	Parameter Description	Min	Nom	Max	Units	Notes
I_{fw}	Forward bias current	5		300	µA	1
n	Diode ideality factor	1.002	1.008	1.016		2, 3, 4, 5

Notes:

1. *The sourcing current should always be used in forward bias only.*
2. *Characterized at 95°C with a forward bias current pair of 10 µA and 100 µA.*
3. *Not 100% tested. Specified by design and limited characterization.*
4. *The diode ideality factor, n, is a correction factor to the ideal diode equation.*

   For the following equations, use the following variables and constants:

   n *Diode ideality factor*
   k *Boltzmann constant*
   q *Electron charge constant*
   T *Diode temperature (Kelvin)*
   V_{BE} *Voltage from base to emitter*
   I_C *Collector current*
   I_S *Saturation current*
   N *Ratio of collector currents*

   The equation for V_{BE} is:

$$V_{BE} = \frac{nkT}{q} \cdot \ln\left(\frac{I_C}{I_S}\right)$$

   By sourcing two currents and using the above equation, a difference in base emitter voltage can be found that leads to the following equation for temperature:

$$T = \frac{\Delta V_{BE}}{n \cdot \ln(N) \cdot \frac{k}{q}}$$

5. *If a different sourcing current pair is used other than 10 µA and 100 µA, the following equation should be used to correct the temperature. Subtract this offset from the temperature measured by the temperature sensor.*

   For the following equations, use the following variables and constants:

   I_{high} *High sourcing current*
   I_{low} *Low sourcing current*

   T_{offset} (in °C) can be found using the following equation:

$$T_{offset} = (6.0 \cdot 10^4) \cdot \frac{(I_{high} - I_{low})}{\ln\left(\frac{I_{high}}{I_{low}}\right)} - 2.34$$

Thermal Protection Characterization. The following section describes parameters relating to thermal protection. The implementation of thermal control circuitry to control processor temperature is left to the manufacturer to determine how to implement.

Thermal limits in motherboard design are necessary to protect the processor from thermal damage. $T_{SHUTDOWN}$ is the temperature for thermal protection circuitry to initiate shutdown of the processor. T_{SD_DELAY} is the maximum time allowed from the detection of the over-temperature condition to processor shutdown to prevent thermal damage to the processor.

Systems that do not implement thermal protection circuitry or that do not react within the time specified by T_{SD_DELAY} can cause thermal damage to the processor during the unlikely events of fan failure or powering up the processor without a heat-sink. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event.

Thermal protection circuitry reference designs and thermal solution guidelines are found in the following documents:

- *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363
- *Thermal Diode Monitoring Circuits*, order# 25658
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794
- http://www1.amd.com/products/athlon/thermals

Mobile specific thermal documentation:

- *Measuring Processor and system Power in a Mobile System*, order# 24353
- *Mobile System Thermal Design Guide*, order# 24383
- *Measuring Temperature on AMD Athlon™ and AMD Duron™ Pin Grid Array Processors with and without an On-Die Thermal Diode*, order#24228

Table 18 shows the $T_{SHUTDOWN}$ and T_{SD_DELAY} specifications for circuitry in motherboard design necessary for thermal protection of the processor.

Table 18. Guidelines for Platform Thermal Protection of the Processor

Symbol	Parameter Description	Max	Units	Notes
$T_{SHUTDOWN}$	Thermal diode shutdown temperature for processor protection	125	°C	1, 2, 3
T_{SD_DELAY}	Maximum allowed time from $T_{SHUTDOWN}$ detection to processor shutdown	500	ms	1, 3

Notes:

1. *The thermal diode is not 100% tested, it is specified by design and limited characterization.*
2. *The thermal diode is capable of responding to thermal events of 40°C/s or faster.*
3. *The mobile AMD Duron™ processor model 7 provides a thermal diode for measuring die temperature of the processor. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event. Refer to* Thermal Diode Monitoring Circuits, order# 25658, *for thermal protection circuitry designs.*

7.16 Reserved Pins DC Characteristics

Table 19 shows the DC characteristics of the Reserved (RSVD) pins.

Table 19. Reserved Pins (N1, N3, and N5) DC Characteristics

Symbol	Parameter Description	Min	Max	Units	Note
I_{LEAK_P}	Tristate Leakage Pullup	–250		µA	*
I_{LEAK_N}	Tristate Leakage Pulldown		250	µA	*

Note:
* *Measured at 2.5 V*

7.17 FID_Change Induced PLL Lock Time

Table 20 shows the time required for the PLL of the processor to lock at the new frequency specified in a FID_Change transition.

Software must program the SGTC field of the FidVidCtl MSR to produce a FID_Change duration equal to or greater than the FID_Change induced PLL lock time.

For more information about the FID_Change protocol, see "Power Management" on page 9.

Table 20. FID_Change Induced PLL Lock Time

Parameter Description	Max	Units
FID_Change Induced PLL Lock Time	50	µs

8 Signal and Power-Up Requirements

This chapter describes the mobile AMD Duron™ processor model 7 power-up requirements during system power-up and warm resets.

8.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 13 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

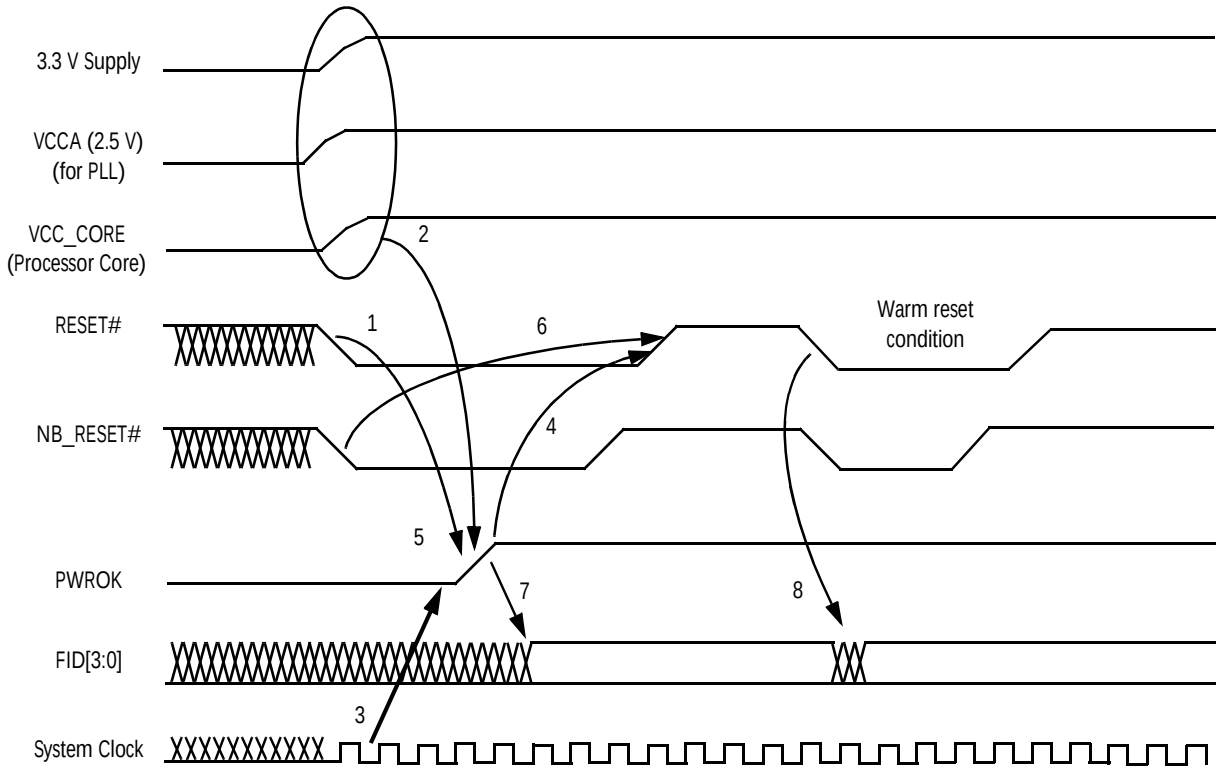


Figure 13. Signal Relationship Requirements During Power-Up Sequence

Notes:

1. *Figure 13 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*
2. *Requirements 1–8 in Figure 13 are described in "Power-Up Timing Requirements" on page 54.*

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.
   The mobile AMD Duron™ processor model 7 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 nanoseconds** prior to the assertion of PWROK.
   In practice, Southbridges will assert RESET# milliseconds before PWROK is deasserted.
2. All motherboard voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC_CORE and all other voltage planes in the system are within specification.

   The motherboard is required to delay PWROK assertion for a minimum of 3 milliseconds from the 3.3 V supply being within specification. This ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, VCC_CORE, must be within specification before PWROK is asserted as dictated by the VID[4:0] pins strapped on the processor package. Before PWROK assertion, the processor is clocked by a ring oscillator. Before PWROK is asserted, the SOFTVID[4:0] outputs of the processor are not driven to a deterministic value. The processor drives the SOFTVID[4:0] outputs to the same value as dictated by the VID[4:0] pins within 20 nanoseconds of PWROK assertion.

   The processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within specification at least 5 microseconds before PWROK is asserted.

   In practice VCCA, VCC_CORE, and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

   After PWROK is asserted, the processor PLL locks to its operational frequency.
3. The system clock (SYSCLK/SYSCLK#) must be running before PWROK is asserted.

When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock must be valid at this time. The system clocks are guaranteed to be running after 3.3 V has been within specification for 3 milliseconds.

4. PWROK assertion to deassertion of RESET#

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1 ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 milliseconds**. Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic and meet the timing requirements as defined in Table 16, "General AC and DC Characteristics," on page 45. The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

   If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer. There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

7. The FID[3:0] signals are valid within 100 ns after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

8. The FID[3:0] signals become valid within 100 ns after RESET# is asserted. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

Clock Multiplier Selection (FID[3:0])

The chipset samples the FID[3:0] signals in a chipset-specific manner from the processor and uses this information to determine the correct Serial Initialization Packet (SIP). The chipset then sends the SIP information to the processor for configuration of the AMD Duron system bus for the clock multiplier that determines the processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, that are synchronous to SYSCLK.

For more information, seeSee “FID[3:0] Pins” on page 79.

Serial Initialization Packet (SIP) Protocol. Refer to *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

8.2 Processor Warm Reset Requirements

Mobile AMD Duron™ Processor Model 7 and Northbridge Reset Pins

RESET# cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. Southbridges enforce a minimum assertion of RESET# for the processor, Northbridge, and PCI of 1.5 to 2.0 milliseconds.

9 Mechanical Data

9.1 Introduction

The mobile AMD Duron processor model 7 connects to the motherboard through a CPGA socket named Socket A. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

9.2 Die Loading

The processor die on the CPGA package is exposed at the top of the package. This is done to facilitate heat transfer from the die to an approved heat sink. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 21. Any heat sink design should avoid loads on corners and edges of die. The CPGA package has compliant pads that serve to bring surfaces in planar contact.

Table 21. CPGA Mechanical Loading[1]

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	2
Die Edge	10	10	lbf	3

Notes:

1. *Tool-assisted zero insertion force sockets should be designed such that no load is placed on the ceramic substrate of the package.*
2. *Load specified for coplanar contact to die surface.*
3. *Load defined for a surface at no more than a two degree angle of inclination to die surface.*

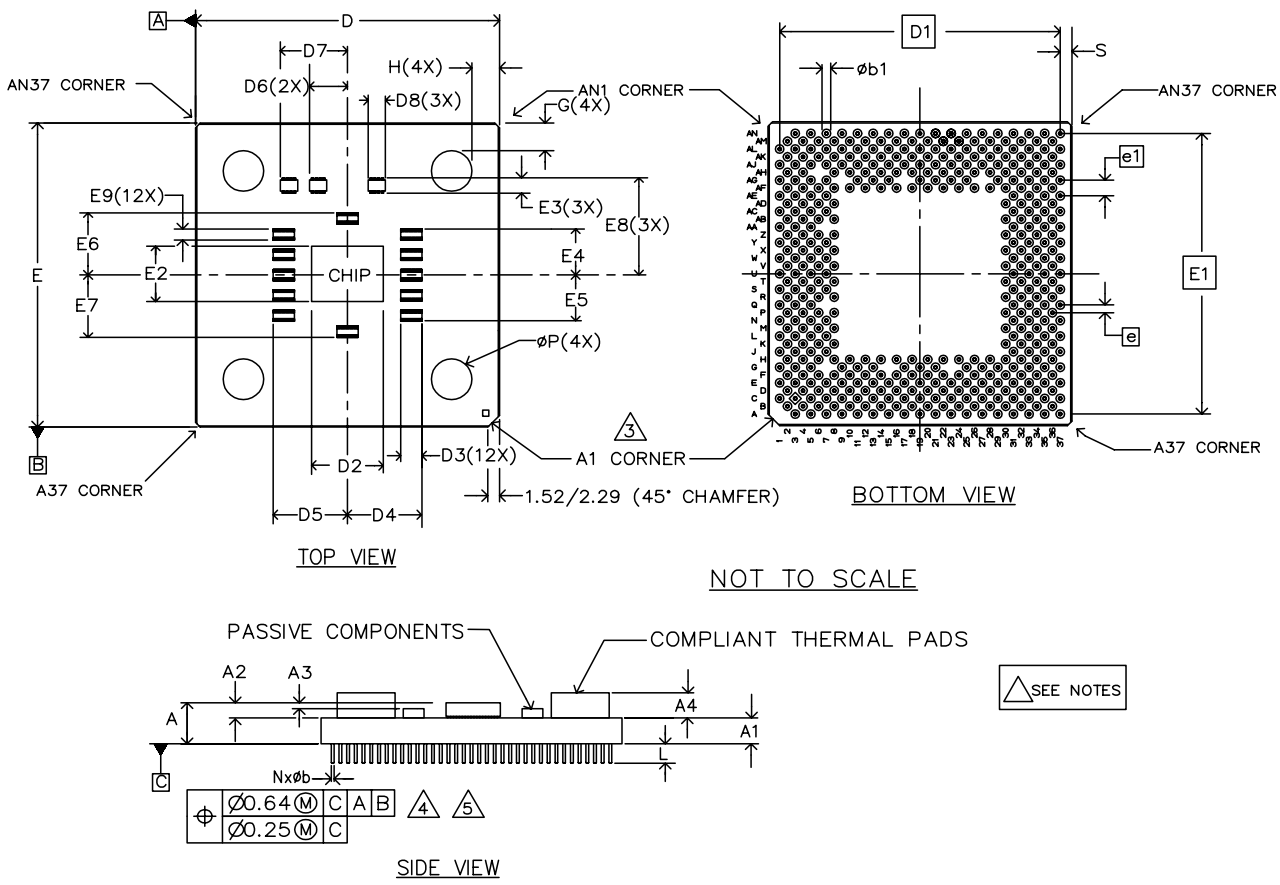
9.3 Package Description

Figure 14 on page 59 shows the mechanical drawing of the CPGA package. Table 22 provides the dimensions in millimeters assigned to the letters and symbols shown in the Figure 14 diagram.

Table 22. Dimensions for the CPGA Package

Letter or Symbol	Minimum Dimension[1]	Maximum Dimension[1]	Letter or Symbol	Minimum Dimension[1]	Maximum Dimension[1]
D/E	49.27	49.78	E9	1.66	1.96
D1/E1	45.72 BSC		G/H	—	4.50
D2	11.698 REF		A	2.24 REF	
D3	3.30	3.60	A1	1.27	1.53
D4	11.84	12.39	A2	0.80	0.88
D5	11.84	12.39	A3	0.116	—
D6	5.91	6.46	A4	—	1.90
D7	10.65	11.20	ϕP	—	6.60
D8	3.05	3.35	ϕb	0.43	0.50
E2	9.034 REF		ϕb1	1.40 REF	
E3	2.35	2.65	S	1.435	2.375
E4	7.25	7.80	L	3.05	3.31
E5	7.25	7.80	M	37	
E6	8.86	9.41	N	453 (pins)	
E7	8.86	9.41	e	1.27 BSC	
E8	15.59	16.38	e1	2.54 BSC	

Note:
1. Dimensions are given in millimeters.



GENERAL NOTES:

1. All dimensions are specified in millimeter (mm).
2. Dimensioning and tolerancing per ASME—Y14.5M—1994.
3. This corner has a chamfer, and is marked with a square on top of the package to identify the pin A1 corner for handling and orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. For staggered pin configuration, pins on the same row are on a 2.54 mm grid. Adjacent rows offset by 1.27 mm.

Figure 14. Mobile AMD Duron™ Processor Model 7 CPGA Package

10 Pin Descriptions

10.1 Pin Diagram and Pin Name Abbreviations

Figure 15 on page 62 shows the staggered pin grid array (SPGA) for the mobile AMD Duron processor model 7. Because some of the pin names are too long to fit in the grid, they are abbreviated. Table 23 on page 64 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

Figure 15. Mobile AMD Duron™ Processor Model 7 Pin Diagram—Topside View

Figure 16. Mobile AMD Duron™ Processor Model 7 Pin Diagram—Bottomside View

Table 23. Pin Name Abbreviations

Abbreviation	Full Name	Pin
	A20M#	AE1
	AMD	AH6
ANLOG	ANALOG	AJ13
CLKFR	CLKFWDRST	AJ21
	CLKIN	AN17
	CLKIN#	AL17
CNNCT	CONNECT	AL23
	COREFB	AG11
	COREFB#	AG13
CPR#	CPU_PRESENCE#	AK6
	DBRDY	AA1
	DBREQ#	AA3
	FERR	AG1
	FID[0]	W1
	FID[1]	W3
	FID[2]	Y1
	FID[3]	Y3
	FLUSH#	AL3
	IGNNE#	AJ1
	INIT#	AJ3
	INTR	AL1
K7CO	K7CLKOUT	AL21
K7CO#	K7CLKOUT#	AN21
	KEY	G7
	KEY	G9
	KEY	G15
	KEY	G17
	KEY	G23
	KEY	G25
	KEY	N7
	KEY	Q7
	KEY	Y7
	KEY	AA7
	KEY	AG7
	KEY	AG9
	KEY	AG15
	KEY	AG17
	KEY	AG27
	KEY	AG29

Abbreviation	Full Name	Pin
	NC	A19
	NC	A31
	NC	C13
	NC	E25
	NC	E33
	NC	F30
	NC	G11
	NC	G13
	NC	G19
	NC	G21
	NC	G27
	NC	G29
	NC	G31
	NC	H28
	NC	H30
	NC	H32
	NC	J5
	NC	J31
	NC	K30
	NC	L31
	NC	L35
	NC	N31
	NC	Q31
	NC	S31
	NC	U31
	NC	U37
	NC	W7
	NC	W31
	NC	Y5
	NC	Y31
	NC	Y33
	NC	AA5
	NC	AA31
	NC	AC7
	NC	AC31
	NC	AD8
	NC	AD30
	NC	AE7
	NC	AE31

Table 23. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
	NC	AF6
	NC	AF8
	NC	AF10
	NC	AF28
	NC	AF30
	NC	AF32
	NC	AG5
	NC	AG19
	NC	AG21
	NC	AG23
	NC	AG25
	NC	AG31
	NC	AH8
	NC	AH30
	NC	AJ7
	NC	AJ9
	NC	AJ11
	NC	AJ15
	NC	AJ17
	NC	AJ19
	NC	AJ27
	NC	AK8
	NC	AL7
	NC	AL9
	NC	AL11
	NC	AL25
	NC	AL27
	NC	AM8
	NC	AN7
	NC	AN9
	NC	AN11
	NC	AN25
	NC	AN27
	NMI	AN3
PLBYP#	PLLBYPASS#	AJ25
PLBYC	PLLBYPASSCLK	AN15
PLBYC#	PLLBYPASSCLK#	AL15
PLMN1	PLLMON1	AN13
PLMN2	PLLMON2	AL13

Abbreviation	Full Name	Pin
PLTST#	PLLTEST#	AC3
PRCRDY	PROCREADY	AN23
	PWROK	AE3
	RSVD	N1
	RSVD	N3
	RSVD	N5
	RESET#	AG3
RCLK	RSTCLK	AN19
RCLK#	RSTCLK#	AL19
SAI#0	SADDIN[0]#	AJ29
SAI#1	SADDIN[1]#	AL29
SAI#2	SADDIN[2]#	AG33
SAI#3	SADDIN[3]#	AJ37
SAI#4	SADDIN[4]#	AL35
SAI#5	SADDIN[5]#	AE33
SAI#6	SADDIN[6]#	AJ35
SAI#7	SADDIN[7]#	AG37
SAI#8	SADDIN[8]#	AL33
SAI#9	SADDIN[9]#	AN37
SAI#10	SADDIN[10]#	AL37
SAI#11	SADDIN[11]#	AG35
SAI#12	SADDIN[12]#	AN29
SAI#13	SADDIN[13]#	AN35
SAI#14	SADDIN[14]#	AN31
SAIC#	SADDINCLK#	AJ33
SAO#0	SADDOUT[0]#	J1
SAO#1	SADDOUT[1]#	J3
SAO#2	SADDOUT[2]#	C7
SAO#3	SADDOUT[3]#	A7
SAO#4	SADDOUT[4]#	E5
SAO#5	SADDOUT[5]#	A5
SAO#6	SADDOUT[6]#	E7
SAO#7	SADDOUT[7]#	C1
SAO#8	SADDOUT[8]#	C5
SAO#9	SADDOUT[9]#	C3
SAO#10	SADDOUT[10]#	G1
SAO#11	SADDOUT[11]#	E1
SAO#12	SADDOUT[12]#	A3
SAO#13	SADDOUT[13]#	G5

Table 23. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SAO#14	SADDOUT[14]#	G3	SD#33	SDATA[33]#	E29
SAOC#	SADDOUTCLK#	E3	SD#34	SDATA[34]#	A27
SCNCK1	SCANCLK1	S1	SD#35	SDATA[35]#	A25
SCNCK2	SCANCLK2	S5	SD#36	SDATA[36]#	E21
SCNINV	SCANINTEVAL	S3	SD#37	SDATA[37]#	C23
SCNSN	SCANSHIFTEN	Q5	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27
SD#28	SDATA[28]#	L37	SDIC#3	SDATAINCLK[3]#	E15
SD#29	SDATA[29]#	J37	SDINV#	SDATAINVALID#	AN33
SD#30	SDATA[30]#	A37	SDOC#0	SDATAOUTCLK[0]#	AE35
SD#31	SDATA[31]#	E35	SDOC#1	SDATAOUTCLK[1]#	C37
SD#32	SDATA[32]#	E31	SDOC#2	SDATAOUTCLK[2]#	A33

Table 23. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SDOC#3	SDATAOUTCLK[3]#	C11	VCC	VCC_CORE	F28
SDOV#	SDATAOUTVALID#	AL31	VCC	VCC_CORE	F32
SFILLV#	SFILLVALID#	AJ31	VCC	VCC_CORE	F34
	SMI#	AN5	VCC	VCC_CORE	F36
SVID[0]	SOFTVID[0]	F8	VCC	VCC_CORE	H2
SVID[1]	SOFTVID[1]	K8	VCC	VCC_CORE	H4
SVID[2]	SOFTVID[2]	H6	VCC	VCC_CORE	H12
SVID[3]	SOFTVID[3]	H8	VCC	VCC_CORE	H16
SVID[4]	SOFTVID[4]	H10	VCC	VCC_CORE	H20
STPC#	STPCLK#	AC1	VCC	VCC_CORE	H24
	TCK	Q1	VCC	VCC_CORE	K32
	TDI	U1	VCC	VCC_CORE	K34
	TDO	U5	VCC	VCC_CORE	K36
THDA	THERMDA	S7	VCC	VCC_CORE	M2
THDC	THERMDC	U7	VCC	VCC_CORE	M4
	TMS	Q3	VCC	VCC_CORE	M6
	TRST#	U3	VCC	VCC_CORE	M8
VCC	VCC_CORE	B4	VCC	VCC_CORE	P30
VCC	VCC_CORE	B8	VCC	VCC_CORE	P32
VCC	VCC_CORE	B12	VCC	VCC_CORE	P34
VCC	VCC_CORE	B16	VCC	VCC_CORE	P36
VCC	VCC_CORE	B20	VCC	VCC_CORE	R2
VCC	VCC_CORE	B24	VCC	VCC_CORE	R4
VCC	VCC_CORE	B28	VCC	VCC_CORE	R6
VCC	VCC_CORE	B32	VCC	VCC_CORE	R8
VCC	VCC_CORE	B36	VCC	VCC_CORE	T30
VCC	VCC_CORE	D2	VCC	VCC_CORE	T32
VCC	VCC_CORE	D4	VCC	VCC_CORE	T34
VCC	VCC_CORE	D8	VCC	VCC_CORE	T36
VCC	VCC_CORE	D12	VCC	VCC_CORE	V2
VCC	VCC_CORE	D16	VCC	VCC_CORE	V4
VCC	VCC_CORE	D20	VCC	VCC_CORE	V6
VCC	VCC_CORE	D24	VCC	VCC_CORE	V8
VCC	VCC_CORE	D28	VCC	VCC_CORE	X30
VCC	VCC_CORE	D32	VCC	VCC_CORE	X32
VCC	VCC_CORE	F12	VCC	VCC_CORE	X34
VCC	VCC_CORE	F16	VCC	VCC_CORE	X36
VCC	VCC_CORE	F20	VCC	VCC_CORE	Z2
VCC	VCC_CORE	F24	VCC	VCC_CORE	Z4

Table 23. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
VCC	VCC_CORE	Z6
VCC	VCC_CORE	Z8
VCC	VCC_CORE	AB30
VCC	VCC_CORE	AB32
VCC	VCC_CORE	AB34
VCC	VCC_CORE	AB36
VCC	VCC_CORE	AD2
VCC	VCC_CORE	AD4
VCC	VCC_CORE	AD6
VCC	VCC_CORE	AF14
VCC	VCC_CORE	AF18
VCC	VCC_CORE	AF22
VCC	VCC_CORE	AF26
VCC	VCC_CORE	AF34
VCC	VCC_CORE	AF36
VCC	VCC_CORE	AH2
VCC	VCC_CORE	AH4
VCC	VCC_CORE	AH10
VCC	VCC_CORE	AH14
VCC	VCC_CORE	AH18
VCC	VCC_CORE	AH22
VCC	VCC_CORE	AH26
VCC	VCC_CORE	AJ5
VCC	VCC_CORE	AK10
VCC	VCC_CORE	AK14
VCC	VCC_CORE	AK18
VCC	VCC_CORE	AK22
VCC	VCC_CORE	AK26
VCC	VCC_CORE	AK30
VCC	VCC_CORE	AK34
VCC	VCC_CORE	AK36
VCC	VCC_CORE	AL5
VCC	VCC_CORE	AM2
VCC	VCC_CORE	AM10
VCC	VCC_CORE	AM14
VCC	VCC_CORE	AM18
VCC	VCC_CORE	AM22
VCC	VCC_CORE	AM26
VCC	VCC_CORE	AM30

Abbreviation	Full Name	Pin
VCC	VCC_CORE	AM34
	VCCA	AJ23
	VID[0]	L1
	VID[1]	L3
	VID[2]	L5
	VID[3]	L7
	VID[4]	J7
VREF_S	VREF_SYS	W5
	VSS	B2
	VSS	B6
	VSS	B10
	VSS	B14
	VSS	B18
	VSS	B22
	VSS	B26
	VSS	B30
	VSS	B34
	VSS	D6
	VSS	D10
	VSS	D14
	VSS	D18
	VSS	D22
	VSS	D26
	VSS	D30
	VSS	D34
	VSS	D36
	VSS	F2
	VSS	F4
	VSS	F6
	VSS	F10
	VSS	F14
	VSS	F18
	VSS	F22
	VSS	F26
	VSS	H14
	VSS	H18
	VSS	H22
	VSS	H26
	VSS	H34

Table 23. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
	VSS	H36
	VSS	K2
	VSS	K4
	VSS	K6
	VSS	M30
	VSS	M32
	VSS	M34
	VSS	M36
	VSS	P2
	VSS	P4
	VSS	P6
	VSS	P8
	VSS	R30
	VSS	R32
	VSS	R34
	VSS	R36
	VSS	T2
	VSS	T4
	VSS	T6
	VSS	T8
	VSS	V30
	VSS	V32
	VSS	V34
	VSS	V36
	VSS	X2
	VSS	X4
	VSS	X6
	VSS	X8
	VSS	Z30
	VSS	Z32
	VSS	Z34
	VSS	Z36
	VSS	AB2
	VSS	AB8
	VSS	AB4
	VSS	AB6
	VSS	AD32
	VSS	AD34
	VSS	AD36

Abbreviation	Full Name	Pin
	VSS	AF12
	VSS	AF16
	VSS	AF2
	VSS	AF20
	VSS	AF24
	VSS	AH16
	VSS	AH34
	VSS	AF4
	VSS	AH12
	VSS	AH20
	VSS	AH24
	VSS	AH28
	VSS	AH32
	VSS	AH36
	VSS	AK2
	VSS	AK4
	VSS	AK12
	VSS	AK16
	VSS	AK20
	VSS	AK24
	VSS	AK28
	VSS	AK32
	VSS	AM4
	VSS	AM6
	VSS	AM12
	VSS	AM16
	VSS	AM20
	VSS	AM24
	VSS	AM28
	VSS	AM32
	VSS	AM36
	ZN	AC5
	ZP	AE5

10.2 Pin List

Table 24 cross-references Socket A pin location to signal name.

The "L" (Level) column shows the electrical specification for this pin. "P" indicates a push-pull mode driven by a single source. "O" indicates open-drain mode that allows devices to share the pin.

Note: *Socket A AMD Duron processors support push-pull drivers. For more information, see "Push-Pull (PP) Drivers" on page 6.*

The "P" (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The "R" (Reference) column indicates if this signal should be referenced to VSS (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths. The "–" is used to indicate that this description is not applicable for this pin.

Table 24. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R
A1	No Pin	page 80	–	–	–
A3	SADDOUT[12]#		P	O	G
A5	SADDOUT[5]#		P	O	G
A7	SADDOUT[3]#		P	O	G
A9	SDATA[55]#		P	B	P
A11	SDATA[61]#		P	B	P
A13	SDATA[53]#		P	B	G
A15	SDATA[63]#		P	B	G
A17	SDATA[62]#		P	B	G
A19	NC Pin	page 80	-	-	-
A21	SDATA[57]#		P	B	G
A23	SDATA[39]#		P	B	G
A25	SDATA[35]#		P	B	P
A27	SDATA[34]#		P	B	P
A29	SDATA[44]#		P	B	G
A31	NC Pin	page 80	-	-	-
A33	SDATAOUTCLK[2]#		P	O	P

Pin	Name	Description	L	P	R
A35	SDATA[40]#		P	B	G
A37	SDATA[30]#		P	B	P
B2	VSS		–	-	-
B4	VCC_CORE		-	-	-
B6	VSS		-	-	-
B8	VCC_CORE		-	-	-
B10	VSS		-	-	-
B12	VCC_CORE		-	-	-
B14	VSS		-	-	-
B16	VCC_CORE		-	-	-
B18	VSS		-	-	-
B20	VCC_CORE		-	-	-
B22	VSS		-	-	-
B24	VCC_CORE		-	-	-
B26	VSS		-	-	-
B28	VCC_CORE		-	-	-
B30	VSS		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
B32	VCC_CORE		-	-	-	D26	VSS		-	-	-
B34	VSS		-	-	-	D28	VCC_CORE		-	-	-
B36	VCC_CORE		-	-	-	D30	VSS		-	-	-
C1	SADDOUT[7]#		P	O	G	D32	VCC_CORE		-	-	-
C3	SADDOUT[9]#		P	O	G	D34	VSS		-	-	-
C5	SADDOUT[8]#		P	O	G	D36	VSS		-	-	-
C7	SADDOUT[2]#		P	O	G	E1	SADDOUT[11]#		P	O	P
C9	SDATA[54]#		P	B	P	E3	SADDOUTCLK#		P	O	G
C11	SDATAOUTCLK[3]#		P	O	G	E5	SADDOUT[4]#		P	O	P
C13	NC Pin	page 80	-	-	-	E7	SADDOUT[6]#		P	O	G
C15	SDATA[51]#		P	B	P	E9	SDATA[52]#		P	B	P
C17	SDATA[60]#		P	B	G	E11	SDATA[50]#		P	B	P
C19	SDATA[59]#		P	B	G	E13	SDATA[49]#		P	B	G
C21	SDATA[56]#		P	B	G	E15	SDATAINCLK[3]#		P	I	G
C23	SDATA[37]#		P	B	P	E17	SDATA[48]#		P	B	P
C25	SDATA[47]#		P	B	G	E19	SDATA[58]#		P	B	G
C27	SDATA[38]#		P	B	G	E21	SDATA[36]#		P	B	P
C29	SDATA[45]#		P	B	G	E23	SDATA[46]#		P	B	P
C31	SDATA[43]#		P	B	G	E25	NC Pin	page 80	-	-	-
C33	SDATA[42]#		P	B	G	E27	SDATAINCLK[2]#		P	I	G
C35	SDATA[41]#		P	B	G	E29	SDATA[33]#		P	B	P
C37	SDATAOUTCLK[1]#		P	O	G	E31	SDATA[32]#		P	B	P
D2	VCC_CORE		-	-	-	E33	NC Pin	page 80	-	-	-
D4	VCC_CORE		-	-	-	E35	SDATA[31]#		P	B	P
D6	VSS		-	-	-	E37	SDATA[22]#		P	B	G
D8	VCC_CORE		-	-	-	F2	VSS		-	-	-
D10	VSS		-	-	-	F4	VSS		-	-	-
D12	VCC_CORE		-	-	-	F6	VSS		-	-	-
D14	VSS		-	-	-	F8	SOFTVID[0]	page 81	O	O	-
D16	VCC_CORE		-	-	-	F10	VSS		-	-	-
D18	VSS		-	-	-	F12	VCC_CORE		-	-	-
D20	VCC_CORE		-	-	-	F14	VSS		-	-	-
D22	VSS		-	-	-	F16	VCC_CORE		-	-	-
D24	VCC_CORE		-	-	-	F18	VSS		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
F20	VCC_CORE		-	-	-	H14	VSS		-	-	-
F22	VSS		-	-	-	H16	VCC_CORE		-	-	-
F24	VCC_CORE		-	-	-	H18	VSS		-	-	-
F26	VSS		-	-	-	H20	VCC_CORE		-	-	-
F28	VCC_CORE		-	-	-	H22	VSS		-	-	-
F30	NC Pin	page 80	-	-	-	H24	VCC_CORE		-	-	-
F32	VCC_CORE		-	-	-	H26	VSS		-	-	-
F34	VCC_CORE		-	-	-	H28	NC Pin	page 80	-	-	-
F36	VCC_CORE		-	-	-	H30	NC Pin	page 80	-	-	-
G1	SADDOUT[10]#		P	O	P	H32	NC Pin	page 80	-	-	-
G3	SADDOUT[14]#		P	O	G	H34	VSS		-	-	-
G5	SADDOUT[13]#		P	O	G	H36	VSS		-	-	-
G7	Key Pin	page 80	-	-	-	J1	SADDOUT[0]#	page 81	P	O	-
G9	Key Pin	page 80	-	-	-	J3	SADDOUT[1]#	page 81	P	O	-
G11	NC Pin	page 80	-	-	-	J5	NC Pin	page 80	-	-	-
G13	NC Pin	page 80	-	-	-	J7	VID[4]	page 81	O	O	-
G15	Key Pin	page 80	-	-	-	J31	NC Pin	page 80	-	-	-
G17	Key Pin	page 80	-	-	-	J33	SDATA[19]#		P	B	G
G19	NC Pin	page 80	-	-	-	J35	SDATAINCLK[1]#		P	I	P
G21	NC Pin	page 80	-	-	-	J37	SDATA[29]#		P	B	P
G23	Key Pin	page 80	-	-	-	K2	VSS		-	-	-
G25	Key Pin	page 80	-	-	-	K4	VSS		-	-	-
G27	NC Pin	page 80	-	-	-	K6	VSS		-	-	-
G29	NC Pin	page 80	-	-	-	K8	SOFTVID[1]	page 81	O	O	-
G31	NC Pin	page 80	-	-	-	K30	NC Pin	page 80	-	-	-
G33	SDATA[20]#		P	B	G	K32	VCC_CORE		-	-	-
G35	SDATA[23]#		P	B	G	K34	VCC_CORE		-	-	-
G37	SDATA[21]#		P	B	G	K36	VCC_CORE		-	-	-
H2	VCC_CORE		-	-	-	L1	VID[0]	page 81	O	O	-
H4	VCC_CORE		-	-	-	L3	VID[1]	page 81	O	O	-
H6	SOFTVID[2]	page 81	O	O	-	L5	VID[2]	page 81	O	O	-
H8	SOFTVID[3]	page 81	O	O	-	L7	VID[3]	page 81	O	O	-
H10	SOFTVID[4]	page 81	O	O	-	L31	NC Pin	page 80	-	-	-
H12	VCC_CORE		-	-	-	L33	SDATA[26]#		P	B	P

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
L35	NC Pin	page 80	-	-	-	R2	VCC_CORE		-	-	-
L37	SDATA[28]#		P	B	P	R4	VCC_CORE		-	-	-
M2	VCC_CORE		-	-	-	R6	VCC_CORE		-	-	-
M4	VCC_CORE		-	-	-	R8	VCC_CORE		-	-	-
M6	VCC_CORE		-	-	-	R30	VSS		-	-	-
M8	VCC_CORE		-	-	-	R32	VSS		-	-	-
M30	VSS		-	-	-	R34	VSS		-	-	-
M32	VSS		-	-	-	R36	VSS		-	-	-
M34	VSS		-	-	-	S1	SCANCLK1	page 81	P	I	-
M36	VSS		-	-	-	S3	SCANINTEVAL	page 81	P	I	-
N1	RSVD	page 80	-	-	-	S5	SCANCLK2	page 81	P	I	-
N3	RSVD	page 80	-	-	-	S7	THERMDA	page 83	-	-	-
N5	RSVD	page 80	-	-	-	S31	NC Pin	page 80	-	-	-
N7	Key Pin	page 80	-	-	-	S33	SDATA[7]#		P	B	G
N31	NC Pin	page 80	-	-	-	S35	SDATA[15]#		P	B	P
N33	SDATA[25]#		P	B	P	S37	SDATA[6]#		P	B	G
N35	SDATA[27]#		P	B	P	T2	VSS		-	-	-
N37	SDATA[18]#		P	B	G	T4	VSS		-	-	-
P2	VSS		-	-	-	T6	VSS		-	-	-
P4	VSS		-	-	-	T8	VSS		-	-	-
P6	VSS		-	-	-	T30	VCC_CORE		-	-	-
P8	VSS		-	-	-	T32	VCC_CORE		-	-	-
P30	VCC_CORE		-	-	-	T34	VCC_CORE		-	-	-
P32	VCC_CORE		-	-	-	T36	VCC_CORE		-	-	-
P34	VCC_CORE		-	-	-	U1	TDI	page 79	P	I	-
P36	VCC_CORE		-	-	-	U3	TRST#	page 79	P	I	-
Q1	TCK	page 79	P	I	-	U5	TDO	page 79	P	O	-
Q3	TMS	page 79	P	I	-	U7	THERMDC	page 83	-	-	-
Q5	SCANSHIFTEN	page 81	P	I	-	U31	NC Pin	page 80	-	-	-
Q7	Key Pin	page 80	-	-	-	U33	SDATA[5]#		P	B	G
Q31	NC Pin	page 80	-	-	-	U35	SDATA[4]#		P	B	G
Q33	SDATA[24]#		P	B	P	U37	NC Pin	page 80	-	-	-
Q35	SDATA[17]#		P	B	G	V2	VCC_CORE		-	-	-
Q37	SDATA[16]#		P	B	G	V4	VCC_CORE		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
V6	VCC_CORE		-	-	-	Z30	VSS		-	-	-
V8	VCC_CORE		-	-	-	Z32	VSS		-	-	-
V30	VSS		-	-	-	Z34	VSS		-	-	-
V32	VSS		-	-	-	Z36	VSS		-	-	-
V34	VSS		-	-	-	AA1	DBRDY	page 79	P	O	-
V36	VSS		-	-	-	AA3	DBREQ#	page 79	P	I	-
W1	FID[0]	page 79	O	O	-	AA5	NC Pin	page 80	-	-	-
W3	FID[1]	page 79	O	O	-	AA7	Key Pin	page 80	-	-	-
W5	VREF_SYS	page 83	P	-	-	AA31	NC Pin	page 80	-	-	-
W7	NC Pin	page 80	-	-	-	AA33	SDATA[8]#		P	B	P
W31	NC Pin	page 80	-	-	-	AA35	SDATA[0]#		P	B	G
W33	SDATAINCLK[0]#		P	I	G	AA37	SDATA[13]#		P	B	G
W35	SDATA[2]#		P	B	G	AB2	VSS		-	-	-
W37	SDATA[1]#		P	B	P	AB4	VSS		-	-	-
X2	VSS		-	-	-	AB6	VSS		-	-	-
X4	VSS		-	-	-	AB8	VSS		-	-	-
X6	VSS		-	-	-	AB30	VCC_CORE		-	-	-
X8	VSS		-	-	-	AB32	VCC_CORE		-	-	-
X30	VCC_CORE		-	-	-	AB34	VCC_CORE		-	-	-
X32	VCC_CORE		-	-	-	AB36	VCC_CORE		-	-	-
X34	VCC_CORE		-	-	-	AC1	STPCLK#	page 81	P	I	-
X36	VCC_CORE		-	-	-	AC3	PLLTEST#	page 80	P	I	-
Y1	FID[2]	page 79	O	O	-	AC5	ZN	page 83	P	-	-
Y3	FID[3]	page 79	O	O	-	AC7	NC Pin	page 80	-	-	-
Y5	NC Pin	page 80	-	-	-	AC31	NC Pin	page 80	-	-	-
Y7	Key Pin	page 80	-	-	-	AC33	SDATA[10]#		P	B	P
Y31	NC Pin	page 80	-	-	-	AC35	SDATA[14]#		P	B	G
Y33	NC Pin	page 80	-	-	-	AC37	SDATA[11]#		P	B	G
Y35	SDATA[3]#		P	B	G	AD2	VCC_CORE		-	-	-
Y37	SDATA[12]#		P	B	P	AD4	VCC_CORE		-	-	-
Z2	VCC_CORE		-	-	-	AD6	VCC_CORE		-	-	-
Z4	VCC_CORE		-	-	-	AD8	NC Pin	page 80	-	-	-
Z6	VCC_CORE		-	-	-	AD30	NC Pin	page 80	-	-	-
Z8	VCC_CORE		-	-	-	AD32	VSS		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AD34	VSS		-	-	-	AG13	COREFB#	page 78	-	-	-
AD36	VSS		-	-	-	AG15	Key Pin	page 80	-	-	-
AE1	A20M#		P	I	-	AG17	Key Pin	page 80	-	-	-
AE3	PWROK		P	I	-	AG19	NC Pin	page 80	-	-	-
AE5	ZP	page 83	P	-	-	AG21	NC Pin	page 80	-	-	-
AE7	NC Pin	page 80	-	-	-	AG23	NC Pin	page 80	-	-	-
AE31	NC Pin	page 80	-	-	-	AG25	NC Pin	page 80	-	-	-
AE33	SADDIN[5]#		P	I	G	AG27	Key Pin	page 80	-	-	-
AE35	SDATAOUTCLK[0]#		P	O	P	AG29	Key Pin	page 80	-	-	-
AE37	SDATA[9]#		P	B	G	AG31	NC Pin	page 80	-	-	-
AF2	VSS		-	-	-	AG33	SADDIN[2]#		P	I	G
AF4	VSS		-	-	-	AG35	SADDIN[11]#		P	I	G
AF6	NC Pin	page 80	-	-	-	AG37	SADDIN[7]#		P	I	P
AF8	NC Pin	page 80	-	-	-	AH2	VCC_CORE		-	-	-
AF10	NC Pin	page 80	-	-	-	AH4	VCC_CORE		-	-	-
AF12	VSS		-	-	-	AH6	AMD Pin	page 78	-	-	-
AF14	VCC_CORE		-	-	-	AH8	NC Pin	page 80	-	-	-
AF16	VSS		-	-	-	AH10	VCC_CORE		-	-	-
AF18	VCC_CORE		-	-	-	AH12	VSS		-	-	-
AF20	VSS		-	-	-	AH14	VCC_CORE		-	-	-
AF22	VCC_CORE		-	-	-	AH16	VSS		-	-	-
AF24	VSS		-	-	-	AH18	VCC_CORE		-	-	-
AF26	VCC_CORE		-	-	-	AH20	VSS		-	-	-
AF28	NC Pin	page 80	-	-	-	AH22	VCC_CORE		-	-	-
AF30	NC Pin	page 80	-	-	-	AH24	VSS		-	-	-
AF32	NC Pin	page 80	-	-	-	AH26	VCC_CORE		-	-	-
AF34	VCC_CORE		-	-	-	AH28	VSS		-	-	-
AF36	VCC_CORE		-	-	-	AH30	NC Pin	page 80	-	-	-
AG1	FERR	page 79	P	O	-	AH32	VSS		-	-	-
AG3	RESET#		-	I	-	AH34	VSS		-	-	-
AG5	NC Pin	page 80	-	-	-	AH36	VSS		-	-	-
AG7	Key Pin	page 80	-	-	-	AJ1	IGNNE#	page 79	P	I	-
AG9	Key Pin	page 80	-	-	-	AJ3	INIT#	page 79	P	I	-
AG11	COREFB	page 78	-	-	-	AJ5	VCC_CORE		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AJ7	NC Pin	page 80	-	-	-	AL1	INTR	page 79	P	I	-
AJ9	NC Pin	page 80	-	-	-	AL3	FLUSH#	page 79	P	I	-
AJ11	NC Pin	page 80	-	-	-	AL5	VCC_CORE		-	-	-
AJ13	Analog	page 78	-	-	-	AL7	NC Pin	page 80	-	-	-
AJ15	NC Pin	page 80	-	-	-	AL9	NC Pin	page 80	-	-	-
AJ17	NC Pin	page 80	-	-	-	AL11	NC Pin	page 80	-	-	-
AJ19	NC Pin	page 80	-	-	-	AL13	PLLMON2	page 80	O	O	-
AJ21	CLKFWDRST	page 78	P	I	P	AL15	PLLBYPASSCLK#	page 80	P	I	-
AJ23	VCCA	page 83	-	-	-	AL17	CLKIN#	page 78	P	I	P
AJ25	PLLBYPASS#	page 80	P	I	-	AL19	RSTCLK#	page 78	P	I	P
AJ27	NC Pin	page 80	-	-	-	AL21	K7CLKOUT	page 80	P	O	-
AJ29	SADDIN[0]#	page 81	P	I	-	AL23	CONNECT	page 78	P	I	P
AJ31	SFILLVALID#		P	I	G	AL25	NC Pin	page 80	-	-	-
AJ33	SADDINCLK#		P	I	G	AL27	NC Pin	page 80	-	-	-
AJ35	SADDIN[6]#		P	I	P	AL29	SADDIN[1]#	page 81	P	I	-
AJ37	SADDIN[3]#		P	I	G	AL31	SDATAOUTVALID#		P	O	P
AK2	VSS		-	-	-	AL33	SADDIN[8]#		P	I	P
AK4	VSS		-	-	-	AL35	SADDIN[4]#		P	I	G
AK6	CPU_PRESENCE#	page 78	-	-	-	AL37	SADDIN[10]#		P	I	G
AK8	NC Pin	page 80	-	-	-	AM2	VCC_CORE		-	-	-
AK10	VCC_CORE		-	-	-	AM4	VSS		-	-	-
AK12	VSS		-	-	-	AM6	VSS		-	-	-
AK14	VCC_CORE		-	-	-	AM8	NC Pin	page 80	-	-	-
AK16	VSS		-	-	-	AM10	VCC_CORE		-	-	-
AK18	VCC_CORE		-	-	-	AM12	VSS		-	-	-
AK20	VSS		-	-	-	AM14	VCC_CORE		-	-	-
AK22	VCC_CORE		-	-	-	AM16	VSS		-	-	-
AK24	VSS		-	-	-	AM18	VCC_CORE		-	-	-
AK26	VCC_CORE		-	-	-	AM20	VSS		-	-	-
AK28	VSS		-	-	-	AM22	VCC_CORE		-	-	-
AK30	VCC_CORE		-	-	-	AM24	VSS		-	-	-
AK32	VSS		-	-	-	AM26	VCC_CORE		-	-	-
AK34	VCC_CORE		-	-	-	AM28	VSS		-	-	-
AK36	VCC_CORE		-	-	-	AM30	VCC_CORE		-	-	-

Table 24. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AM32	VSS		-	-	-
AM34	VCC_CORE		-	-	-
AM36	VSS		-	-	-
AN1	No Pin	page 80	-	-	-
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 80	-	-	-
AN9	NC Pin	page 80	-	-	-
AN11	NC Pin	page 80	-	-	-
AN13	PLLMON1	page 80	O	B	-
AN15	PLLBYPASSCLK	page 80	P	I	-
AN17	CLKIN	page 78	P	I	P
AN19	RSTCLK	page 78	P	I	P
AN21	K7CLKOUT#	page 80	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 80	-	-	-
AN27	NC Pin	page 80	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

10.3 Detailed Pin Descriptions

The information in this section pertains to Table 23 on page 64 and Table 24 on page 70.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

AMD Duron™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

Analog Pin

Treat this pin as a NC.

CLKFWDRST Pin

CLKFWDRST resets clock-forward circuitry for both the system and processor.

CLKIN and RSTCLK (SYSCLK) Pins

Connect CLKIN (AN17) with RSTCLK (AN19) and name it SYSCLK. Connect CLKIN# (AL17) with RSTCLK# (AL19) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.

See “SYSCLK and SYSCLK#” on page 83 for more information.

CONNECT Pin

CONNECT is an input from the system used for power management and clock-forward initialization at reset.

COREFB and COREFB# Pins

COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.

CPU_PRESENCE# Pin

CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor.

DBRDY and DBREQ# Pins

DBRDY (AA1) and DBREQ# (AA3) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.

FERR Pin

FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

The FID[3:0] pins drive a value of:

```
FID[3:0] = 0 1 0 0
```

that corresponds to a 5x SYSCLK multiplier after PWROK is asserted to the processor. This information is used by the Northbridge to create the SIP stream that the Northbridge sends to the processor after RESET# is deasserted.

For more information, see "SYSCLK Multipliers" on page 24 and "Frequency Identification (FID[3:0])" on page 35 for the AC and DC characteristics for FID[3:0].

FLUSH# Pin

FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.

IGNNE# Pin

IGNNE# is an input from the system that tells the processor to ignore numeric errors.

INIT# Pin

INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.

INTR Pin

INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.

JTAG Pins

TCK (Q1), TMS (Q3), TDI (U1), TRST# (U3), and TDO (U5) are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE with pullup resistors.

K7CLKOUT and K7CLKOUT# Pins

K7CLKOUT (AL21) and K7CLKOUT# (AN21) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.

Key Pins

These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.

NC Pins

The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

NMI Pin

NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins

No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.

For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

PLL Bypass and Test Pins

PLLTEST# (AC3), PLLBYPASS# (AJ25), PLLMON1 (AN13), PLLMON2 (AL13), PLLBYPASSCLK (AN15), and PLLBYPASSCLK# (AL15) are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

PWROK Pin

The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.

For more information, see “Signal and Power-Up Requirements” on page 53.

RSVD Pins

Reserved pins (N1, N3, and N5) must have pulldown resistors to ground on the motherboards.

SADDIN[1:0]# and SADDOUT[1:0]# Pins

The mobile AMD Duron processor model 7 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models of the mobile AMD Duron processors may support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

Scan Pins

SCANSHIFTEN (Q5), SCANCLK1 (S1), SCANINTEVAL (S3), and SCANCLK2 (S5) are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.

SMI# Pin

SMI# is an input that causes the processor to enter the system management mode.

SOFTVID[4:0] and VID[4:0] Pins

The VID[4:0] (Voltage ID) and SOFTVID[4:0] (Software driven Voltage ID) outputs are used by the DC to DC power converter to select the processor core voltage. The VID[4:0] pins are strapped to ground or left unconnected on the package and must be pulled up on the motherboard. The SOFTVID[4:0] pins are open drain and 2.5-V tolerant. The SOFTVID[4:0] pins of the processor must not be pulled to voltages higher than 2.5 V.

The motherboard is required to implement a VID multiplexer to select a deterministic voltage for the processor at power–up before the PWROK input is asserted. Before PWROK is asserted, the VID multiplexer drives the VID value from VID[4:0] pins to the DC to DC converter for VCC_CORE. After PWROK is asserted, the VID multiplexer drives the VID value from the SOFTVID[4:0] pins to the DC to DC converter for VCC_CORE of the processor. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363 for the recommended VID multiplexer circuit.

The SOFTVID[4:0] pins are driven by the processor to select the maximum VCC_CORE of the processor as reported by the Maximum VID field of the FidVidStatus MSR within 20 ns of PWROK assertion. Before PWROK is asserted, the SOFTVID[4:0] outputs are not driven to a deterministic value. The SOFTVID[4:0] outputs must be used to select VCC_CORE after PWROK is asserted. Any time the RESET# input is asserted, the SOFTVID[4:0] pins will be driven to select the maximum voltage.

Note: *The Start–up VID and Maximum VID fields of the FidVidStatus MSR report the same value that corresponds to the nominal voltage that the processor requires to operate at maximum frequency.*

AMD PowerNow!™ technology can use the FID_Change protocol described in Section on page 9 to transition the SOFTVID[4:0] outputs and therefore VCC_CORE as part of processor performance state transitions.

The VID codes used by the mobile AMD Duron processor model 7 are defined in Table 25.

Note: *VID codes for the mobile AMD Duron processors are different from the VID codes for the desktop AMD Duron processors.*

Table 25. SOFTVID[4:0] and VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE (V)	VID[4:0]	VCC_CORE (V)
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	Shutdown	11111	Shutdown

STPCLK# Pin

STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.

SYSCLK and SYSCLK# SYSCLK and SYSCLK# are differential input clock signals provided to the processor's PLL from a system-clock generator. See "CLKIN and RSTCLK (SYSCLK) Pins" on page 78 for more information.

THERMDA and THERMDC Pins Thermal Diode anode (THERMDA) and cathode (THERMDC) pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system. See Table 17 on page 48 for more details.

VCCA Pin VCCA is the processor PLL supply. For information about the VCCA pin, see Table 7, "VCCA AC and DC Characteristics," on page 35 and the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

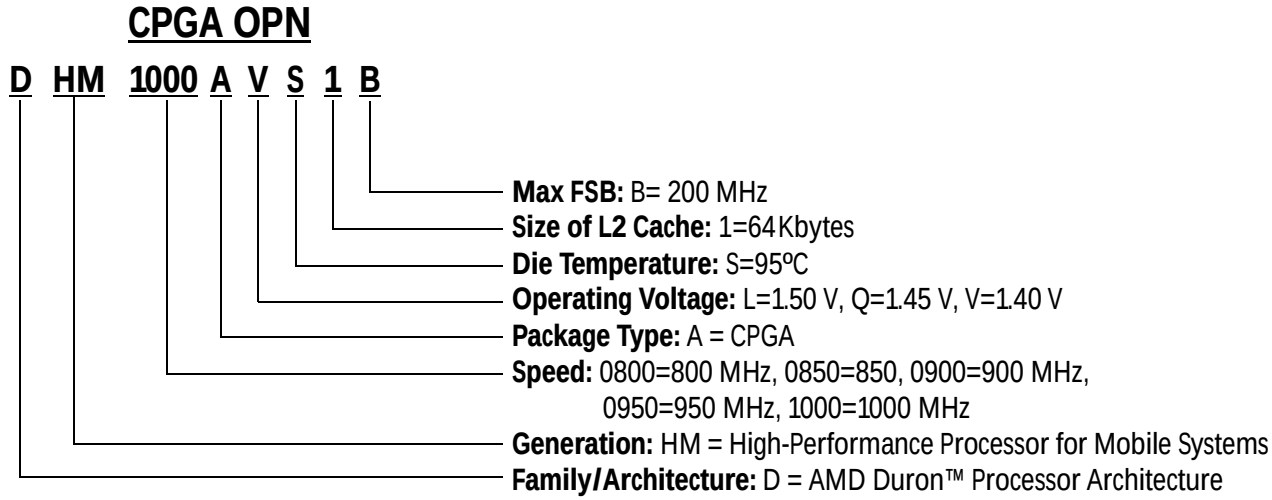
VREF_SYS Pin VREF_SYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREF_SYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREF_SYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

ZN and ZP Pins ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z_0 of the transmission line.

11 Ordering Information

11.1 Standard Mobile AMD Duron™ Processor Model 7 Products

AMD standard products are available in several operating ranges. The ordering part number (OPN) is formed by a combination of the elements shown in Figure 17. ***This OPN is given as an example only.***



Note: Spaces are added to the number shown above for viewing clarity only.

Figure 17. OPN Example for the Mobile AMD Duron™ Processor Model 7

Appendix A

Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don’t-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - A mobile AMD Duron processor model 7 cache line is eight quadwords (64 bytes)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 26 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 26 contains the definitions of abbreviations used in this document.

Table 26. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga–
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo–
Kbyte	Kilobyte
M	Mega–
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli–
ms	Millisecond
mW	Milliwatt
µ	Micro–
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano–
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
pF	picofarad
pH	picohenry
ps	picosecond

Table 26. Abbreviations (continued)

Abbreviation	Meaning
s	Second
V	Volt
W	Watt

Table 27 contains the definitions of acronyms used in this document.

Table 27. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CPGA	Ceramic Pin Grid Array
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor to Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers

Table 27. Acronyms (continued)

Abbreviation	Meaning
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OBGA	Organic Ball Grid Array
OD	Open Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor to Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer

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The following books discuss various aspects of computer architecture that may enhance your understanding of AMD products:

AMD Publications

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